High-Definition Multimedia Interface (HDMI) Intel FPGA IP Release Notes
# Contents

1. Intel FPGA HDMI IP Release Notes

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<td>HDMI IP Core v14.1</td>
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1. Intel FPGA HDMI IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the Intel® Quartus® Prime Design Suite Update Release Notes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Introduction to Intel FPGA IP Cores
- HDMI Intel FPGA IP User Guide
  Refer to the HDMI Intel FPGA IP Design Example User Guide Archives section for previous versions.
- HDMI Intel Arria 10 FPGA IP Design Example User Guide
  Refer to the HDMI Intel Arria 10 FPGA IP Design Example User Guide Archives section for previous versions.
- HDMI Intel Cyclone 10 GX IP FPGA Design Example User Guide
  Refer to the HDMI Intel Cyclone 10 GX FPGA IP Design Example User Guide Archives section for previous versions.
- HDMI Intel Stratix 10 FPGA IP Design Example User Guide
  Refer to the HDMI Intel Stratix 10 FPGA IP Design Example User Guide Archives section for previous versions.
- Errata for HDMI Intel FPGA IP in the Knowledge Base

1.1. HDMI Intel FPGA IP v19.1

<table>
<thead>
<tr>
<th>Table 1. v19.1 April 2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
</tr>
<tr>
<td>---------------------------------</td>
</tr>
<tr>
<td>Enabled final support for Intel Stratix® 10 L-tile and H-tile devices. The design examples now target Intel Stratix 10 production devices.</td>
</tr>
</tbody>
</table>

1.2. HDMI Intel FPGA IP v18.1 Update 1

18.1.1 December 2018

- For Intel Stratix 10 H-Tile devices, added VID_OPERATION_MODE "PMBUS MASTER" and PWRMGMNT settings to the video connectivity design example IP .qsf file to enable Intel Stratix 10 SmartVID and power management capabilities.

Related Information

- Introduction to Intel FPGA IP Cores
## 1.3. HDMI Intel FPGA IP v18.1

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Improved the HDMI RX video lock time for HDMI 2.0 for Intel Stratix 10 design examples.</td>
<td>These changes are optional. If you do not upgrade your IP core, it does not have these new features.</td>
</tr>
<tr>
<td>Added support for Bitec HDMI FMC daughter card revision 11 in the Intel Arria® 10, Intel Cyclone® 10 GX, and Intel Stratix 10 design examples.</td>
<td></td>
</tr>
</tbody>
</table>

### Related Information
- Introduction to Intel FPGA IP Cores
- HDMI Intel FPGA IP User Guide
- HDMI Intel Arria 10 FPGA Design Example User Guide
- HDMI Intel Cyclone 10 GX FPGA Design Example User Guide
- HDMI Intel Stratix 10 FPGA Design Example User Guide
- Errata for HDMI Intel FPGA IP in the Knowledge Base

## 1.4. HDMI Intel FPGA IP v18.0

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Renamed Intel FPGA HDMI IP to HDMI Intel FPGA IP as part of standardizing and rebranding exercise.</td>
<td>–</td>
</tr>
<tr>
<td>Added preliminary support for Intel Stratix 10 (H-Tile) devices.</td>
<td>The Intel Stratix 10 devices are only available in the Intel Quartus Prime Pro Edition software.</td>
</tr>
<tr>
<td>Updated the HDMI Intel FPGA IP to support HDMI Specification 2.0b.</td>
<td>These changes are optional. If you do not upgrade your IP core, it does not have these new features.</td>
</tr>
<tr>
<td>Added support for Xcelium® Parallel simulator.</td>
<td>–</td>
</tr>
<tr>
<td>Added the following files:</td>
<td></td>
</tr>
<tr>
<td>• xcelium_files.tcl</td>
<td></td>
</tr>
<tr>
<td>• xcelium_setup.sh</td>
<td></td>
</tr>
<tr>
<td>• xcelium_sim.sh</td>
<td></td>
</tr>
<tr>
<td>Added support for SCDC read request feature in the HDMI RX core.</td>
<td></td>
</tr>
<tr>
<td>Added final support for Intel Cyclone 10 GX devices.</td>
<td>The Intel Cyclone 10 GX devices are only available in the Intel Quartus Prime Pro Edition software.</td>
</tr>
<tr>
<td>Added new design examples for Intel Cyclone 10 GX devices in version 17.1.1 release. Refer to the HDMI Intel Cyclone 10 GX FPGA IP Design Example User Guide for more information.</td>
<td></td>
</tr>
</tbody>
</table>
Table 4. **Design Files Required for IP Upgrade**

The implementation of the IP on hardware requires additional components specific to the device targeted. These additional components, such as Native PHY, TX PLL, reconfiguration controller, are not included as part of the Intel Quartus Prime IP Upgrade flow. Upgrading an IP core would require the inclusion of these files generated as part of the IP design example.

<table>
<thead>
<tr>
<th>Design Example</th>
<th>Required Files</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel Arria 10</td>
<td>• quartus\a10_hDMI2_demo.qsf</td>
</tr>
<tr>
<td></td>
<td>• rtl\gxb\gxb_tx_fpll.qsys—regenerate before you compile in the Intel Quartus Prime software.</td>
</tr>
<tr>
<td></td>
<td>• rtl\hdmi_rx\hdmi_rx_top.v</td>
</tr>
<tr>
<td></td>
<td>• rtl\hdmi_rx\mr_hdmi_rx_core_top.v</td>
</tr>
<tr>
<td></td>
<td>• rtl\reconfig_mgmt\mr_reconfig_mgmt.v</td>
</tr>
<tr>
<td></td>
<td>• rtl\sdc\a10_hDMI2.sdc</td>
</tr>
<tr>
<td></td>
<td>• rtl\a10_hDMI2_demo.v</td>
</tr>
<tr>
<td>Intel Cyclone 10 GX</td>
<td>• quartus\c10_hDMI2_demo.qsf</td>
</tr>
<tr>
<td></td>
<td>• rtl\sdc\c10_hDMI2.sdc</td>
</tr>
<tr>
<td></td>
<td>• sdc\mr_clock_sync.sdc</td>
</tr>
<tr>
<td></td>
<td>• rtl\sdc\mr_reconfig_mgmt.sdc</td>
</tr>
<tr>
<td></td>
<td>• rtl\sdc\rxtx_link.sdc</td>
</tr>
<tr>
<td></td>
<td>• rtl\c10_hDMI2_demo.v</td>
</tr>
<tr>
<td></td>
<td>• rtl\xcvr_transceiver_arbiter.v</td>
</tr>
</tbody>
</table>

**Related Information**

- Introduction to Intel FPGA IP Cores
- HDMI Intel FPGA IP User Guide
- HDMI Intel Arria 10 FPGA Design Example User Guide
- HDMI Intel Cyclone 10 GX FPGA Design Example User Guide
- HDMI Intel Stratix 10 FPGA Design Example User Guide
- Errata for HDMI Intel FPGA IP in the Knowledge Base

### 1.5. **Intel FPGA HDMI IP Core v17.1**

Table 5. **v17.1 November 2017**

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Renamed the following as per Intel rebranding:</td>
<td>–</td>
</tr>
<tr>
<td>• HDMI IP core to Intel FPGA HDMI IP core</td>
<td></td>
</tr>
<tr>
<td>• Qsys to Platform Designer</td>
<td></td>
</tr>
<tr>
<td>The <strong>Support for deep color</strong> parameter is now turned on by default.</td>
<td>–</td>
</tr>
<tr>
<td>Added advance support for Intel Cyclone 10 GX devices.</td>
<td></td>
</tr>
<tr>
<td>The Intel Cyclone 10 GX devices are only available in the Intel Quartus Prime Pro Edition software.</td>
<td></td>
</tr>
</tbody>
</table>

*continued...*
## 1.6. HDMI IP Core v17.0

### Table 6. v17.0 May 2017

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Available in both Quartus Prime Pro Edition and Quartus Prime Standard Edition.</td>
<td>These changes are optional. If you do not upgrade your IP core, it does not have these new features.</td>
</tr>
<tr>
<td>Added demonstration for HDR InfoFrame insertion and filtering.</td>
<td></td>
</tr>
<tr>
<td>Changed to PPLL direct for TX transceiver.</td>
<td></td>
</tr>
<tr>
<td>Enabled TX PMA recalibration.</td>
<td></td>
</tr>
</tbody>
</table>

### Related Information
- Introduction to Intel FPGA IP Cores
- Intel FPGA HDMI User Guide
- Intel FPGA HDMI Design Example User Guide for Intel Arria 10 Devices
- Errata for Intel FPGA HDMI IP Core in the Knowledge Base

## 1.7. HDMI IP Core v16.1

### Table 7. v16.1 October 2016

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>The 16.1 version of the HDMI IP core is available only in Quartus Prime Standard Edition.</td>
<td>These changes are optional. If you do not upgrade your IP core, it does not have these new features.</td>
</tr>
<tr>
<td>Added new Design Example tab in the HDMI IP core parameter editor. The design example is for Arria 10 devices. Refer to the HDMI IP Core Design Example User Guide for more information.</td>
<td></td>
</tr>
<tr>
<td>Changed audio_de port width to 1 bit.</td>
<td></td>
</tr>
</tbody>
</table>

### Related Information
- Introduction to Intel FPGA IP Cores
- High-Definition Multimedia Interface (HDMI) User Guide
- HDMI Design Example User Guide
- Errata for HDMI IP Core in the Knowledge Base

continued...
1.8. HDMI IP Core v16.0

Table 8. v16.0 May 2016

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Added Audio Metadata Packet to comply to HDMI Specification Version 2.0.</td>
<td>These changes are optional. If you do not upgrade your IP core, it does not have these new features.</td>
</tr>
</tbody>
</table>

Added new interface ports:
- HDMI source
  - audio_metadata[164:0]
  - audio_format[4:0]
- HDMI sink
  - audio_metadata[164:0]
  - audio_format[4:0]
  - vid_lock
  - aux_error

Related Information
- Introduction to Intel FPGA IP Cores
- Altera High-Definition Multimedia Interface User Guide
- Errata for HDMI IP Core in the Knowledge Base

1.9. HDMI IP Core v15.1

Table 9. v15.1 November 2015

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Added the following new GUI parameters:</td>
<td>These changes are optional. If you do not upgrade your IP core, it does not have these new features.</td>
</tr>
</tbody>
</table>

continued...
Updated the following interface ports:

- **HDMI source**
  - Added \texttt{ctrl}
  - Removed \texttt{gcp\_Set\_AVMute} and \texttt{gcp\_Clear\_AVMute}

- **HDMI sink**
  - Added \texttt{ctrl}, \texttt{mode}, \texttt{in\_5v\_power}, and \texttt{in\_hp}
  - Removed \texttt{gcp\_Set\_AVMute} and \texttt{gcp\_Clear\_AVMute}

### Related Information

- Introduction to Altera IP Cores
- High-Definition Multimedia Interface (HDMI) User Guide
- Errata for HDMI IP Core in the Knowledge Base

#### 1.10. HDMI IP Core v15.0 Update 1

**Table 10. v15.0 Update 1 June 2015**

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed the timing violation on the oversampling block in the Arria V HDMI 2.0 design.</td>
<td>Upgrade if you are using the Arria V HDMI 2.0 design.</td>
</tr>
</tbody>
</table>

**Related Information**

- Introduction to Altera IP Cores
- High-Definition Multimedia Interface (HDMI) User Guide
- Errata for HDMI IP Core in the Knowledge Base

#### 1.11. HDMI IP Core v15.0

**Table 11. v15.0 May 2015**

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Upgraded support for HDMI specification compliance from version 1.4b to 2.0.</td>
<td>These changes are optional. If you do not upgrade your IP core, it does not have these new features.</td>
</tr>
<tr>
<td>Added 4 symbols per clock.</td>
<td></td>
</tr>
<tr>
<td>Added Status and Control Data Channel (SCDC) for HDMI specification version 2.0.</td>
<td></td>
</tr>
<tr>
<td>Added the following interface ports:</td>
<td>continued...</td>
</tr>
</tbody>
</table>
## HDMI IP Core v14.1

### Table 12. v14.1 December 2014

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial release.</td>
<td>-</td>
</tr>
</tbody>
</table>

**Related Information**

- Introduction to Altera IP Cores
- High-Definition Multimedia Interface (HDMI) User Guide
- Errata for HDMI IP Core in the Knowledge Base