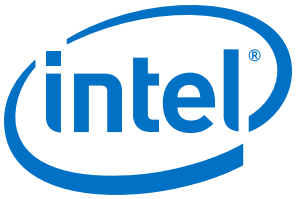

Low Latency 100G Ethernet Intel® Stratix® 10 FPGA IP Core Release Notes

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1. Low Latency 100G Ethernet Intel® Stratix® 10 FPGA IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Intel Quartus Prime Design Suite Update Release Notes*.

Related Information

Intel Quartus Prime Design Suite Update Release Notes

1.1. Low Latency 100G Ethernet Intel® Stratix® 10 FPGA IP Core v18.1

Table 1. Version 18.1

Description	Impact	Notes
Added support for Auto-negotiation (AN) as defined in IEEE Standard 802.3-2015 Clause 73 and the 25G Ethernet Consortium Schedule Draft 1.6.	—	New feature. Use the **AN/LT Options** parameter to enable this feature.
Added support for Link training (LT) as defined in IEEE Standard 802.3-2015 Clauses 92 and 93 and the 25G Ethernet Consortium Schedule Draft 1.6.	—	New feature. Use the **AN/LT Options** parameters to enable this feature.
Added the dynamic control support for RS-FEC bypass capability.	—	—
Added support for Partial Reconfiguration.	—	—

Related Information

- Low Latency 100G Ethernet Intel Stratix 10 FPGA IP Core User Guide
- Intel FPGA Knowledge Base

1.2. Low Latency 100G Ethernet Intel® Stratix® 10 FPGA IP Core v18.0

Table 2. Version 18.0

Description	Impact	Notes
Added support for local fault and remote fault monitoring and statistics.	—	—
Added support for optional IEEE 802.3 Clause 31 Ethernet flow control and priority-based flow control.	—	—
Added support for 322.265625 MHz PHY reference frequency.	—	—

continued...

Description	Impact	Notes
Transceiver reconfiguration clock and control and status interface clock changed from 100 - 125 MHz to 100 - 162 MHz.	—	—
Added parameters for Low Latency 100G Ethernet Intel FPGA IP core: • **Enable MAC Flow Control** - Turning on this parameter enables the flow control mechanism. • **Number of queues in priority flow control** - Number of distinct priority queues for priority-based flow control. • **Enable link fault generation** - Turning on this parameter includes link fault signaling modules and relevant signals.	—	—
Added support for hardware design example generation using Stratix 10 GX Transceiver Signal Integrity Development Kit.	—	—

Related Information

- Low Latency 100G Ethernet Intel Stratix 10 FPGA IP Core User Guide
- Intel FPGA Knowledge Base

1.3. Intel® Stratix® 10 Low Latency 100G Ethernet IP Core v17.1

Table 3. Version 17.1

Description	Impact	Notes
Initial release in the Intel FPGA IP Library.	—	—

Related Information

- Low Latency 100G Ethernet Intel Stratix 10 FPGA IP Core User Guide
- Intel FPGA Knowledge Base