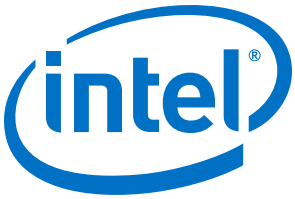

H-Tile Hard IP for Ethernet Intel® Stratix® 10 FPGA IP Core Release Notes

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1. Intel® Stratix® 10 H-Tile Hard IP for Ethernet IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Intel Quartus Prime Design Suite Update Release Notes*.

Related Information

Intel Quartus Prime Design Suite Update Release Notes

1.1. H-Tile Hard IP for Ethernet Intel Stratix 10 FPGA IP Core v18.0

Table 1. Version 18.0 May 2018

Description	Impact	Notes
Added support for Optical Transport Network (OTN) and Flexible Ethernet.	—	—
Added deficit idle counter (DIC) option for more refined inter-packet gap (IPG) control.	—	—
Added the following GUI parameters: • **Link fault generation option** • **Enable asynchronous adapter clock** • **Enable Altera Debug Master Endpoint (ADME)**	—	—
Added simulation design examples for: • 50GE and 100GE OTN variation • 50GE and 10GE FlexE variation	—	—
Added hardware design example for 50GE and 100GE MAC + PCS variant.	—	—

Related Information

- H-Tile Hard IP for Ethernet Intel® Stratix® 10 FPGA IP Core User Guide
- Errata for Intel® Stratix® 10 H-Tile Hard IP for Ethernet IP core in the Knowledge Base

1.2. Intel® Stratix® 10 H-Tile Hard IP for Ethernet IP Core v17.1

Table 2. Version 17.1 November 2017

Description	Impact	Notes
Initial release in the Intel FPGA IP Library.		

Related Information

- Intel® Stratix® 10 H-Tile Hard IP for Ethernet IP Core User Guide
- Errata for Intel® Stratix® 10 H-Tile Hard IP for Ethernet IP core in the Knowledge Base