H-Tile Hard IP for Ethernet Intel® Stratix® 10 FPGA IP Core Release Notes
1. Intel® Stratix® 10 H-Tile Hard IP for Ethernet IP Core Release Notes

   1.1. H-Tile Hard IP for Ethernet Intel Stratix 10 FPGA IP Core v18.0
   1.2. Intel® Stratix® 10 H-Tile Hard IP for Ethernet IP Core v17.1
1. Intel® Stratix® 10 H-Tile Hard IP for Ethernet IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the Intel Quartus Prime Design Suite Update Release Notes.

Related Information
Intel Quartus Prime Design Suite Update Release Notes

1.1. H-Tile Hard IP for Ethernet Intel Stratix 10 FPGA IP Core v18.0

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Added support for Optical Transport Network (OTN) and Flexible Ethernet.</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Added deficit idle counter (DIC) option for more refined inter-packet gap (IPG) control.</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>
| Added the following GUI parameters:  
  - Link fault generation option  
  - Enable asynchronous adapter clock  
  - Enable Altera Debug Master Endpoint (ADME) | — | — |
| Added simulation design examples for:  
  - 50GE and 100GE OTN variation  
  - 50GE and 10GE FlexE variation | — | — |
| Added hardware design example for 50GE and 100GE MAC + PCS variant. | — | — |

Related Information
- H-Tile Hard IP for Ethernet Intel® Stratix® 10 FPGA IP Core User Guide
- Errata for Intel® Stratix® 10 H-Tile Hard IP for Ethernet IP core in the Knowledge Base

1.2. Intel® Stratix® 10 H-Tile Hard IP for Ethernet IP Core v17.1

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial release in the Intel FPGA IP Library.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Related Information
- Intel® Stratix® 10 H-Tile Hard IP for Ethernet IP Core User Guide
- Errata for Intel® Stratix® 10 H-Tile Hard IP for Ethernet IP core in the Knowledge Base

Intel Corporation. All rights reserved. Intel, the Intel logo, Altera, Arria, Cyclone, Enpirion, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel’s standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

*Other names and brands may be claimed as the property of others.*