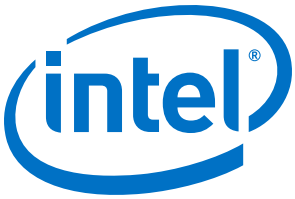

H-Tile Hard IP for Ethernet Intel® Stratix® 10 FPGA IP Core Release Notes

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1. Intel® Stratix® 10 H-Tile Hard IP for Ethernet IP Core Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- H-Tile Hard IP for Ethernet Intel FPGA IP User Guide
- H-Tile Hard IP for Ethernet Intel Stratix® 10 FPGA IP Design Example User Guide

1.1. H-Tile Hard IP for Ethernet Intel Stratix 10 FPGA IP Core v20.2

Table 1. v19.3.0 2020.06.22

Intel Quartus Prime Version	Description	Impact
20.2	The 50GE variation is no longer available in the Intel Quartus Prime Pro Edition software. For more details, contact Intel support.	50G Ethernet rate is not available in the parameter editor.

1.2. H-Tile Hard IP for Ethernet Intel Stratix 10 FPGA IP Core v18.0

Table 2. Version 18.0 May 2018

Description	Impact	Notes
Added support for Optical Transport Network (OTN) and Flexible Ethernet.	—	—
Added deficit idle counter (DIC) option for more refined inter-packet gap (IPG) control.	—	—

continued...

Description	Impact	Notes
Added the following GUI parameters: • **Link fault generation option** • **Enable asynchronous adapter clock** • **Enable Altera Debug Master Endpoint (ADME)**	—	—
Added simulation design examples for: • 50GE and 100GE OTN variation • 50GE and 10GE FlexE variation	—	—
Added hardware design example for 50GE and 100GE MAC + PCS variant.	—	—

Related Information

- H-Tile Hard IP for Ethernet Intel Stratix® 10 FPGA IP Core User Guide
- Errata for Intel Stratix® 10 H-Tile Hard IP for Ethernet IP core in the Knowledge Base

1.3. Intel Stratix® 10 H-Tile Hard IP for Ethernet IP Core v17.1

Table 3. Version 17.1 November 2017

Description	Impact	Notes
Initial release in the Intel FPGA IP Library.		

Related Information

- Intel Stratix® 10 H-Tile Hard IP for Ethernet IP Core User Guide
- Errata for Intel Stratix® 10 H-Tile Hard IP for Ethernet IP core in the Knowledge Base