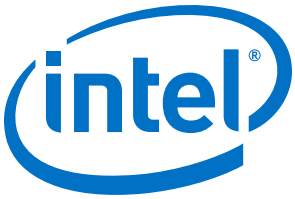

E-Tile Hard IP for Ethernet Release Notes

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Contents

1. E-Tile Hard IP for Ethernet Release Notes

This release notes describe the E-Tile Hard IP for Ethernet content updates for Intel® Stratix® 10 and Intel Agilex™ device family.

Intel Quartus® Prime Design Suite software support **E-Tile Hard IP for Ethernet Intel FPGA IP** for Intel Stratix 10 device family and **E-Tile Ethernet IP for Intel Agilex FPGA** for Intel Agilex device family.

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel Quartus Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP versioning scheme (X.Y.Z) number changes from one software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Introduction to Intel FPGA IP Cores
- E-tile Hard IP for Ethernet and CPRI PHY Intel FPGA IPs User Guide
- E-tile Hard IP Intel Stratix 10 FPGA IP Design Examples User Guide: Ethernet, CPRI PHY, and Dynamic Reconfiguration
- E-tile Hard IP for Ethernet Intel Agilex FPGA IP Design Examples User Guide
- Errata for the E-tile Hard IP for Ethernet Intel FPGA IP in the Knowledge Base

2. E-Tile Hard IP for Ethernet Intel FPGA IP Release Notes

This section describes the content of E-Tile Hard IP for Ethernet Intel FPGA IP updates.

2.1. E-Tile Hard IP for Ethernet Intel FPGA IP v19.3.0

Table 1. v19.3.0 2019.09.30

Intel Quartus Prime Version	Description	Impact
19.3	10G/25G variant for E-tile Hard IP for Ethernet Intel FPGA IP: • UI adjustment under +/-100ppm condition for 10G/25G variants.	The E-tile Hard IP for Ethernet Intel FPGA IP provides set of registers to compute the new TX/RX UI under PPM condition.
	10G/25G variant for E-tile Hard IP for Ethernet Intel FPGA IP: • Added **Ready Latency** parameter for 10GE/ 25GE variants.	Useful when user need to pipeline TX valid signal when facing a timing issue.
	IP tab for E-tile Hard IP for Ethernet Intel FPGA IP: • Removed **Reconfig clock rate** parameter.	—
	Added production device kit support: • Updated the target development kit option for Intel Stratix 10 devices from **Stratix 10 TX Transceiver Signal Integrity Development Kit** to **Stratix 10 TX SI Development Kit -1ST280EY2F55E2VGS1** and **Stratix 10 TX SI Development Kit -1ST280EY2F55E2VG**.	User can select different development kit with different OPN.

2.2. E-Tile Hard IP for Ethernet Intel FPGA IP v19.2

Table 2. v19.2 July 2019

Description	Impact
Added **25G Ethernet to CPRI Protocol** in the Dynamic Reconfiguration Design Example.	—
Removed **Enable asynchronous adapter clocks** parameter in 100G variants.	—
Added support for Ethernet Link Inspector.	—

2.3. E-tile Hard IP for Ethernet Intel FPGA IP v19.1

Table 3. v19.1 April 2019

Description	Impact
Added Custom PCS feature to support generic protocols other than Ethernet. This feature support data rate ranges from 10 to 28 Gbps.	—
Added IEEE 1588 precision time protocol (PTP) support for 100G Ethernet variants.	—
No multichannel support for auto-negotiation with RS-FEC or PTP enabled in 25G variants.	—
Added `i_clk_aib` and `i_clk_aib_2x` clock signals to source clock from user logic. These signals are enabled through **Enable external AIB clocking** parameter.	—
Removed support for asynchronous adapter clocks feature.	Selecting **Enable asynchronous adapter clocks** parameter does not provide any asynchronous clocks functionality in the IP.
Added simulation, compilation-only, and hardware design examples for the following variants: • Custom PCS with optional RS-FEC • 100G Ethernet with IEEE 1588 PTP	—

2.4. E-Tile Hard IP for Ethernet Intel FPGA IP v18.1.1

Table 4. v18.1.1 December 2018

Description	Impact
Added **PMA Adaptation** parameters to customize E-tile transceiver PMA calibration after power-on.	—
Added `o_sl_rx_pcs_fully_aligned` (10G/25G)/ `o_rx_pcs_fully_aligned`(100G) signals to determine link fault condition.	—
Added design examples with PMA calibration for 100G variant.	—
Removed hardware design examples for the following variants: • 10GE/25GE OTN with optional RS-FEC and PTP • 10GE/25GE FlexE with optional RS-FEC and PTP	—

Related Information

- Introduction to Intel FPGA IP Cores
- E-Tile Hard IP for Ethernet Intel FPGA IP User Guide
- Errata for the E-Tile Hard IP for Ethernet Intel FPGA IP in the Knowledge Base

2.5. E-Tile Hard IP for Ethernet Intel FPGA IP v18.1

Table 5. v18.1 September 2018

Description	Impact
Added support for 10GE/25GE with optional Reed-Solomon Forward Error Correction (RS-FEC) with Auto-Negotiation and Link Training variant up to 4 channels.	—
Added support for Auto-Negotiation and Link Training with the following features: • Optional RSFEC request during Auto-Negotiation • Option to advertise copper cable (CR) or backplane (KR) capability • Option to select default lane to perform Auto-Negotiation • Option to advertise both 10GE and 25GE capability during Auto-Negotiation • Option to enable symmetric and asymmetric pauses as defined in Annex 28B of Section 2 of IEEE Std 802.3–2015	—
Added support of the following variants for 10GE/25GE: • PCS Only • Optical Transport Network (OTN) • Flexible Ethernet	—
Added Precision Timestamp Protocol (PTP) for 10GE variant.	—
Added 156.250000 MHz PHY Reference Frequency support for 10GE/25GE.	—
Added the following PHY Reference Frequency support for 100GE: • 322.265625 MHz • 312.500000 MHz • 644.531250 MHz	—
Added support for RS-FEC (544,514) coding for 100GE MAC + PCS, PCS only, OTN, and FlexE variants.	—
Added simulation and hardware design examples for the following variants: • 10GE/25GE/100GE MAC + PCS with optional RS-FEC and PTP • 10GE/25GE PCS with optional RS-FEC and PTP • 10GE/25GE OTN with optional RS-FEC and PTP • 10GE/25GE FlexE with optional RS-FEC and PTP • 100GE PCS with optional RS-FEC • 100GE OTN with optional RSF-FEC • 100GE FlexE with optional RS-FEC	—
When there are multiple E-Tile for Hard IP Ethernet IP cores with different configurations instantiated in a project, the design may compile incorrectly or may cause fitter error.	Users will see compilation warning where settings for modules with the same name are overwritten during Quartus project compilation and design simulation compilation. This may also affect the design functionality in simulation and hardware. For more information, refer to Warning (16817): Verilog HDL waring at alt_etipc3_nphy_elane.v (12698)
Fitter is unable to place transceivers correctly when more than 1 channel of 10GE/25GE with PTP and RSFEC enabled, due to incorrect channel restrictions.	Users will observed fitter error during compilation. For more information, refer to Why do I get fitter errors when compiling a design

continued...

Description	Impact
	with multiple instances of the Intel Stratix 10 E-tile Hard IP for Ethernet Intel FPGA IP, where PTP and RSFEC options have been enabled?.
For 100GE PCS+(528,514)RSFEC and 100GE PCS+(544,514)RSFEC variant, there is no signal to indicate local fault condition in the IP core.	The IP core is not able to detect local fault condition on RX PCS datapath. For more information, refer to How do I tell the difference between a local fault condition and valid RX data when using the Intel® Stratix® 10 E-tile Hard IP for Ethernet Intel® FPGA IP configured in PCS+FEC status without the MAC .

Related Information

- Introduction to Intel FPGA IP Cores
- E-Tile Hard IP for Ethernet Intel FPGA IP User Guide
- Errata for the E-Tile Hard IP for Ethernet Intel FPGA IP in the Knowledge Base

2.6. E-Tile Hard IP for Ethernet Intel FPGA IP v18.0

Table 6. v18.0 May 2018

Description	Impact
Initial release in the Intel FPGA IP Library. *Note:* You are not allowed to bypass VID setup in the Intel Quartus Prime software for the VID part because the device function may fail.	–

Related Information

- Introduction to Intel FPGA IP Cores
- E-Tile Hard IP for Ethernet Intel FPGA IP User Guide
- Errata for the E-Tile Hard IP for Ethernet Intel FPGA IP in the Knowledge Base

3. E-Tile Ethernet IP for Intel Agilex FPGA Release Notes

This section describes the content of E-Tile Ethernet IP for Intel Agilex FPGA updates.

3.1. E-Tile Ethernet IP for Intel Agilex FPGA IP v19.3.0

Table 7. v19.3.0 2019.09.30

Intel Quartus Prime Version	Description	Impact
19.3	Initial release for Intel Agilex devices. • Added support for the following variants: — 10GE/25GE/100GE MAC + PCS with optional RS-FEC and PTP — 10GE/25GE PCS with optional RS-FEC — 10GE/25GE OTN with optional RS-FEC — 10GE/25GE FlexE with optional RS-FEC — 100GE PCS with optional RS-FEC — 100GE OTN with optional RSF-FEC — 100GE FlexE with optional RS-FEC	User can compile design and generate a `.sof` file.

4. E-tile Hard IP User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
19.1	Intel FPGA IP User Guide
18.1.1	Intel FPGA IP User Guide
18.0	Intel FPGA IP User Guide