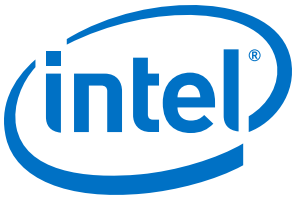

25G Ethernet Intel® FPGA IP Release Notes

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1. 25G Ethernet Intel® FPGA IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP versioning scheme (X.Y.Z) number changes from one software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- 25G Ethernet Intel Arria® 10 FPGA IP User Guide
- 25G Ethernet Intel Arria® 10 FPGA IP Design Example User Guide
- 25G Ethernet Intel Stratix® 10 FPGA IP User Guide Archives
- 25G Ethernet Intel Stratix® 10 FPGA IP Design Example User Guide Archives
- Errata for the 25G Ethernet Intel FPGA IP in the Knowledge Base

1.1. 25G Ethernet Intel FPGA IP v19.2.0

Table 1. v19.2.0 2019.07.01

Intel Quartus Prime Version	Description	Impact
19.2	Design Example for 25G Ethernet Intel FPGA IP: • Updated the target development kit option for Intel Stratix® 10 devices from **Intel Stratix 10 L-Tile GX Transceiver Signal Integrity Development Kit** to **Intel Stratix 10 10 GX Signal Integrity L-Tile (Production) Development Kit**.	—

1.2. 25G Ethernet Intel FPGA IP v19.1

Table 2. v19.1 April 2019

Description	Impact
Added a new feature—Adaptive mode for RX PMA Adaptation: • Added a new parameter—**Enable auto adaptation triggering for RX PMA CTLE/DFE mode**.	These changes are optional. If you do not upgrade your IP core, it does not have this new feature.
Renamed the **Enable Altera Debug Master Endpoint (ADME)** parameter to **Enable Native PHY Debug Master Endpoint (NPDME)** as per Intel rebranding in the Intel Quartus Prime Pro Edition software. The Intel Quartus Prime Standard Edition software still uses **Enable Altera Debug Master Endpoint (ADME)**.	—

1.3. 25G Ethernet Intel FPGA IP v18.1

Table 3. Version 18.1 September 2018

Description	Impact
Added a new feature—Elective PMA: • Added a new parameter—**Core Variants**.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
• Added a new signal for 1588 Precision Time Protocol Interface—`latency_sclk`.	
Design Example for 25G Ethernet Intel FPGA IP: Renamed the target development kit option for Intel Stratix 10 devices from **Stratix 10 GX FPGA Development Kit** to **Stratix 10 L-Tile GX Transceiver Signal Integrity Development Kit**.	—

Related Information

- 25G Ethernet Intel Stratix 10 FPGA IP User Guide
- 25G Ethernet Intel Stratix 10 FPGA IP Design Example User Guide
- Errata for 25G Ethernet IP core in the Knowledge Base

1.4. 25G Ethernet Intel FPGA IP v18.0

Table 4. Version 18.0 May 2018

Description	Impact
Added support for the Intel Stratix 10 device family.	—

Related Information

- 25G Ethernet Intel Stratix 10 FPGA IP User Guide
- 25G Ethernet Intel Stratix 10 FPGA IP Design Example User Guide
- Errata for 25G Ethernet IP core in the Knowledge Base

1.5. 25G Ethernet IP Core v17.0

Table 5. Version 17.0 May 2017

Description	Impact
Added shadow feature for reading statistics registers. • In TX statistics registers, replaced the CLEAR_TX_STATS register at offset 0x845 with new CNTR_TX_CONFIG register. The new register adds a shadow request and a parity-error clear bit to the bit that clears all TX statistics registers. Added new CNTR_RX_STATUS register at offset 0x846, that includes a parity-error bit and a status bit for the shadow request. • In RX statistics registers, replaced the CLEAR_RX_STATS register at offset 0x945 with new CNTR_RX_CONFIG register.The new register adds a shadow request and a parity-error clear bit to the bit that clears all TX statistics registers. Added new CNTR_TX_STATUS register at offset 0x946, that includes a parity-error bit and a status bit for the shadow request.	The new feature supports improved reliability in statistics counter reads. To read a statistics counter, first set the shadow request bit for that set of registers (RX or TX), and then read from a snapshot of the register. The read values stop incrementing while the shadow feature is in effect, but the underlying counters continue to increment. After you reset the request, the counters resume their accumulated values. In addition, the new register fields include parity-error status and clear bits.
Modified RS-FEC alignment marker format to comply with the now-finalized Clause 108 of the IEEE 802.3by specification. Previously the RS-FEC feature complied with the 25G/50G Consortium Schedule 3, prior to IEEE specification finalization.	The RX RS-FEC now detects and locks to both the old and new alignment markers, but the TX RS-FEC generates only the new IEEE alignment marker format.

Related Information

- 25G Ethernet IP Core User Guide
- Errata for 25G Ethernet IP core in the Knowledge Base

1.6. 25G Ethernet IP Core v16.1

Table 6. Version 16.1 October 2016

Description	Impact
Initial release in the Intel FPGA IP Library.	—

Related Information

- 25G Ethernet IP Core User Guide
- Errata for 25G Ethernet IP core in the Knowledge Base

1.7. 25G Ethernet Intel Stratix 10 FPGA IP User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
18.1	25G Ethernet Intel Stratix 10 FPGA IP User Guide
18.0	25G Ethernet Intel Stratix 10 FPGA IP User Guide

1.8. Intel Stratix 10 FPGA IP Design Example User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
19.1	Intel Stratix 10 FPGA IP Design Example User Guide
18.1	Intel Stratix 10 FPGA IP Design Example User Guide
18.0	Intel Stratix 10 FPGA IP Design Example User Guide