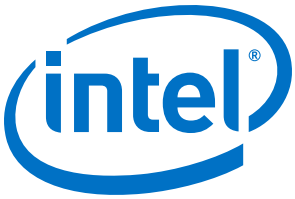

DisplayPort Intel FPGA IP Release Notes

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Contents

1. DisplayPort Intel® FPGA IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Introduction to Intel FPGA IP Cores
- DisplayPort Intel FPGA IP User Guide
  Refer to the DisplayPort Intel FPGA IP User Guide Archives section for previous versions.
- DisplayPort Intel Arria 10 FPGA IP Design Example User Guide
  Refer to the DisplayPort Intel Arria 10 FPGA IP Design Example User Guide Archives section for previous versions.
- DisplayPort Intel Cyclone 10 GX FPGA IP Design Example User Guide
  Refer to the DisplayPort Intel Cyclone 10 GX FPGA IP Design Example User Guide Archives section for previous versions.
- DisplayPort Intel Stratix 10 FPGA IP Design Example User Guide
  Refer to the DisplayPort Intel Stratix 10 FPGA IP Design Example User Guide Archives section for previous versions.
- Errata for DisplayPort Intel FPGA IP in the Knowledge Base

1.1. DisplayPort Intel FPGA IP v19.1

Table 1. v19.1 April 2019

Description	Impact
Enabled final support for Intel Stratix® 10 L-tile and H-tile devices. The design examples now target Intel Stratix 10 production devices.	If you want to target your designs to use Intel Stratix 10 L-tile devices, you must upgrade your IP core.

1.2. DisplayPort Intel FPGA IP v18.1 Update 1

18.1.1 December 2018

- For Intel Stratix 10 devices, enabled Pixel Clock Recovery function.
- Changed Synopsys Design Constraints to entity-based Synopsys Design Constraints.
- Cleaned up compilation warnings found in Intel Stratix 10 design example with pixel clock recovery.
- Enabled Intel Stratix 10 design example with Pixel Clock Recovery variant.

- Enabled initiation of Tx in software regardless of the setting of DP_SUPPORT_EDID_PASSTHRU.
- Fixed an Intel Arria® 10 design example when no display output occurred in non GPU mode.
- Enabled extended receiver capabilities when the maximum link rate is HBR3.
- For Intel Stratix 10 H-tile devices, added VID_OPERATION_MODE "PMBUS MASTER" and PWRMGMT settings to the video connectivity design example IP `.qsf` file to enable Intel Stratix 10 SmartVID and power management capabilities.

Related Information

- Introduction to Intel FPGA IP Cores
- DisplayPort Intel FPGA IP User Guide
- DisplayPort Intel Arria 10 FPGA Design Example User Guide
- DisplayPort Intel Cyclone 10 GX FPGA Design Example User Guide
- DisplayPort Intel Stratix 10 FPGA Design Example User Guide
- Errata for DisplayPort Intel FPGA IP in the Knowledge Base

1.3. DisplayPort Intel FPGA IP v18.1

Table 2. 18.1 September 2018

Description	Impact
Added a new design example for Intel Stratix 10 devices in version 18.1 release. Refer to the *DisplayPort Intel Stratix 10 FPGA IP Design Example User Guide* for more information.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Updated the design examples for Intel Arria 10 devices to support multi stream transport (MST).	

Related Information

- Introduction to Intel FPGA IP Cores
- DisplayPort Intel FPGA IP User Guide
- DisplayPort Intel Arria 10 FPGA Design Example User Guide
- DisplayPort Intel Cyclone 10 GX FPGA Design Example User Guide
- DisplayPort Intel Stratix 10 FPGA Design Example User Guide
- Errata for DisplayPort Intel FPGA IP in the Knowledge Base

1.4. DisplayPort Intel FPGA IP v18.0

Table 3. v18.0 May 2018

Description	Impact
Renamed Intel FPGA DisplayPort IP to DisplayPort Intel FPGA IP as part of standardizing and rebranding exercise.	–
Added support for Xcelium* Parallel simulator.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added the following files: • `xcelium_files.tcl` • `xcelium_setup.sh` • `xcelium_sim.sh`	
Added final support for Intel Cyclone® 10 GX devices.	The Intel Cyclone 10 GX devices are only available in the Intel Quartus Prime Pro Edition software.
Added new design examples for Intel Cyclone 10 GX devices in version 17.1.1 release. Refer to the *DisplayPort Intel Cyclone 10 GX FPGA IP Design Example User Guide* for more information.	

Table 4. Design Files Required for IP Upgrade

The implementation of the IP on hardware requires additional components specific to the device targeted.

These additional components, such as Native PHY, TX PLL, reconfiguration controller, are not included as part of the Intel Quartus Prime IP Upgrade flow. Upgrading an IP core would require the inclusion of these files generated as part of the IP design example.

Design Example	Required Files
Intel Arria 10	• `quartus\a10_dp_demo.qsf` • `rtl\rx_phy\rx_phy_top.v` • `rtl\tx\tx_phy_top.v` • `rtl\a10_dp_demo.v` • `rtl\bitec_reconfig_alt_a10.v` • `rtl\a10_reconfig_arbiter.sv` • `software\main.c` • `software\rx_utils.c` • `software\tx_utils.c` • `software\tx_utils.h` • `software\config.h` Execute `script\build_sw.sh` before project compilation to update Software API and regenerate the software `.elf` file.
Intel Cyclone 10 GX	• `quartus\c10_dp_demo.qsf` • `rtl\rx_phy\rx_phy_top.v` • `rtl\tx\tx_phy_top.v` • `rtl\c10_dp_demo.v` • `rtl\bitec_reconfig_alt_c10.v` • `rtl\c10_reconfig_arbiter.sv` • `software\main.c` • `software\rx_utils.c` • `software\tx_utils.c` • `software\tx_utils.h` • `software\config.h` Execute `script\build_sw.sh` before project compilation to update Software API and regenerate the software `.elf` file.

Related Information

- Introduction to Intel FPGA IP Cores
- DisplayPort Intel FPGA IP User Guide
- DisplayPort Intel Arria 10 FPGA Design Example User Guide
- DisplayPort Intel Cyclone 10 GX FPGA Design Example User Guide
- Errata for DisplayPort Intel FPGA IP in the Knowledge Base

1.5. Intel FPGA DisplayPort IP Core v17.1

Table 5. v17.1 November 2017

Description	Impact
Renamed the following as per Intel rebranding: • DisplayPort IP core to Intel FPGA DisplayPort IP core • Qsys to Platform Designer	–
Added advance support for Intel Cyclone 10 GX devices.	The Intel Cyclone 10 GX devices are only available in the Intel Quartus Prime Pro Edition software.
YCbCr 4:2:0 color format is now supported.	These features are only available in the Intel Quartus Prime Pro Edition software.
The Intel FPGA DisplayPort IP core version 17.1 conforms to *Video Electronics Standards Association (VESA) DisplayPort Standard version 1.4*.	
Added data link rate support for HBR3 (8.10 Gbps). This rate is only available in quad symbols per clock for Intel Arria 10 and Intel Cyclone 10 GX devices. *Note:* The clock recovery module in the Intel Arria 10 design examples only support up to 4Kp60 resolution.	
Updated the design examples to **DisplayPort SST Parallel Loopback With PCR** and **DisplayPort SST Parallel Loopback Without PCR**.	
In previous versions of the DisplayPort Intel FPGA design example for Intel Arria 10 devices, the IOPLL and transceiver PLL output may experience additional jitter. The additional jitter occurs if you source the reference clock from a cascaded PLL output, global clock, or core clock. To compensate for the jitter, the designs require additional constraints. This issue has been fixed in the Intel Quartus Prime software version 17.1.	If you are upgrading designs that have these additional constraints from the previous versions of Intel Quartus Prime to version 17.1, you must revise the constraints. Refer to the KDB page for more information.

Related Information

- Introduction to Intel FPGA IP Cores
- Intel FPGA DisplayPort IP Core User Guide
- Intel FPGA DisplayPort IP Core Design Example User Guide for Intel Arria 10 Devices
- Errata for Intel FPGA DisplayPort IP Core in the Knowledge Base

1.6. DisplayPort IP Core v17.0

Table 6. v17.0 May 2017

Description	Impact
Available in both Quartus Prime Pro Edition and Quartus Prime Standard Edition.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added support for the following features: • Adaptive sync (preliminary) • YCbCr 4:2:0 color format (preliminary) • Proprietary video image format for DisplayPort source	
Added a new parameter: **TX Video IM Enable**. Turn on to enable the video image interface. Turn off to use the traditional HSYNC/ VSYNC/DE video input interface.	
Multi-stream transport (MST) feature supports audio data channel.	

Related Information

- Introduction to Intel FPGA IP Cores
- DisplayPort IP Core User Guide
- DisplayPort IP Core Design Example User Guide
- Errata for DisplayPort IP Core in the Knowledge Base

1.7. DisplayPort IP Core v16.1

Table 7. v16.1 October 2016

Description	Impact
The 16.1 version of the DisplayPort IP core is available only in Quartus Prime Standard Edition.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Multi-stream transport (MST) feature does not support audio data channel.	
Added support for multiple TX instances in software API.	
Added new **Design Example** tab in the DisplayPort IP core parameter editor. The design example is for Arria 10 devices. Refer to the *DisplayPort IP Core Design Example User Guide* for more information.	

Related Information

- Introduction to Intel FPGA IP Cores
- DisplayPort IP Core User Guide
- DisplayPort IP Core Design Example User Guide
- Errata for DisplayPort IP Core in the Knowledge Base

1.8. DisplayPort IP Core v16.0

Table 8. v16.0 May 2016

Description	Impact
Removed the **Import fixed MSA** parameter and the `txN_msa_conduit` signal. The DisplayPort source core now automatically inserts the TX main stream attribute (MSA).	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added support for black video feature for DisplayPort sink core.	
Added support for Link Quality Analysis (LQA).	

Related Information

- Introduction to Intel FPGA IP Cores
- DisplayPort IP Core User Guide
- Errata for DisplayPort IP Core in the Knowledge Base

1.9. DisplayPort IP Core v15.1

Table 9. v15.1 November 2015

Description	Impact
The `txN_vid_f` pin is removed from the DisplayPort IP core. The IP core handles the interface internally.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Updated multi-stream support: • 1, 2, 3, or 4 streams for Arria 10 and Stratix V devices • 1 or 2 streams for Arria V devices	

Related Information

- Introduction to Intel FPGA IP Cores
- DisplayPort IP Core User Guide
- Errata for DisplayPort IP Core in the Knowledge Base

1.10. DisplayPort IP Core v15.0

Table 10. v15.0 May 2015

Description	Impact
Added preliminary support for Arria 10 devices.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Updated color support. • RGB—18, 24, 30, 36, or 48 bpp • YCbCr 4:4:4—24, 30, 36, or 48 bpp • YCbCr 4:2:2—16, 20, 24, or 32 bpp	
Added source-supported DPCD locations.	
Added new bits for `DPTX_TEST_80BIT_PATTERN` bits.	
Removed the Link Quality Generation register bits and combined these bits into the `DPTX_TX_CONTROL` register.	

continued...

Description	Impact
• 0000 = Normal video • 0001 = Training pattern 1 • 0010 = Training pattern 2 • 0011 = Training pattern 3 • 0111 = Video idle pattern • 1001 = D10.2 test pattern (same as training pattern 1) • 1010 = Symbol error rate measurement pattern • 1011 = PRBS7 • 1100 = 80-bit custom pattern • 1101 = HBR2 compliance test pattern (CP2520 pattern 1)	
Added new sink-supported DPCD location bits: `TEST_REQUEST`, `TEST_LINK_RATE`, `TEST_LANE_COUNT`, `PHY_TEST_PATTERN`, and `TEST_80BIT_CUSTOM_PATTERN`.	
Added simulation testbench for Arria 10 devices.	

Related Information

- Introduction to Intel FPGA IP Cores
- DisplayPort IP Core User Guide
- Errata for DisplayPort IP Core in the Knowledge Base

1.11. DisplayPort IP Core v14.1

Table 11. v14.1 December 2014

Description	Impact
Added multi-stream support (MST, 1 to 4 source and sink streams). You can access this feature using these parameters: • **Support MST** • **Max stream count**	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added support for 4Kp60 resolution.	
Removed support for double reference clocks—162 MHz and 270 MHz—for transceiver clocking.	
Updated the design example with pixel clock recovery feature and 4Kp60 support.	
Added new signals.	
Added new source registers: • 0×00a0 (DPTX_MST_CONTROL1) • 0×00a2 (DPTX _MST_VCPTAB0) • 0×00a3 (DPTX _MST_VCPTAB • 0×00a3 (DPTX _MST_VCPTAB1) • 0×00a4 (DPTX _MST_VCPTAB2) • 0×00a5 (DPTX _MST_VCPTAB3) • 0×00a6 (DPTX _MST_VCPTAB4) • 0×00a7 (DPTX _MST_VCPTAB5) • 0×00a8 (DPTX _MST_VCPTAB6) • 0×00a9 (DPTX _MST_VCPTAB7) • 0×00aa (DPTX _MST_TAVG_TS)	
Added new sink registers:	

continued...

Description	Impact
• 0×0006 (DPRX_BER_CNTI0) • 0×0007 (DPRX_BER_CNTI1) • 0×00a0 (DPRX_MST_CONTROL1) • 0×00a1 (DPRX_MST_STATUS1) • 0×00a2 (DPRX _MST_VCPTAB0) • 0×00a3 (DPRX _MST_VCPTAB1) • 0×00a4 (DPRX _MST_VCPTAB2) • 0×00a5 (DPRX _MST_VCPTAB3) • 0×00a6 (DPRX _MST_VCPTAB4) • 0×00a7 (DPRX _MST_VCPTAB5) • 0×00a8 (DPRX _MST_VCPTAB6) • 0×00a9 (DPRX _MST_VCPTAB7)	
Changed the value of the following register bits: • Source register — 0×0000 - Bits RX_LINK_RATE — 0×0001 - Bits RX_LINK_RATE — 0×0002 - Bits RSTI3, RSTI2, RSTI1, RSTI0 • Sink register — 0×0000 - Bits TX_LINK_RATE and ENHANCED_FRAME	

Table 12. DisplayPort IP Core Signal Changes

Signals added or modified in version 14.1.

Old Signal Name	New Signal Name	Notes
—	clk_cal	Calibration clock for transceiver management interface
—	tx_link_rate_8bits	Main link rate expressed in multiples of 270Mbps
—	rx_link_rate_8bits	
—	txN_video_in (N=1,2,3)	TX signals for Stream 1, 2 and 3
—	txN_vid_clk (N=1,2,3)	
—	txN_audio (N=1,2,3)	
—	txN_audio_clk (N=1,2,3)	
—	txN_ss (N=1,2,3)	
—	txN_msa_conduit (N=1,2,3)	
—	rxN_video_out (N=1,2,3)	RX signals for Stream 1, 2 and 3
—	rxN_vid_clk (N=1,2,3)	
—	rxN_audio (N=1,2,3)	
—	rxN_ss (N=1,2,3)	
—	rxN_msa_conduit (N=1,2,3)	
—	rxN_stream (N=1,2,3)	
tx_xcvr_clkout	tx_ss_clk	—
rx_xcvr_clkout	rx_ss_clk	—

Related Information

- Introduction to Intel FPGA IP Cores

- DisplayPort IP Core User Guide
- Errata for DisplayPort IP Core in the Knowledge Base