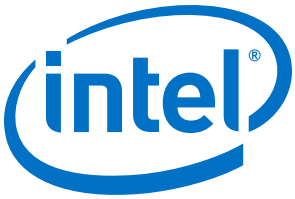

Intel® FPGA SDK for OpenCL™ Standard Edition

Version 18.1 Release Notes

Updated for Intel® Quartus® Prime Design Suite: **18.1**

RN-1154 | 2018.09.24
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1. Intel® FPGA SDK for OpenCL™ Standard Edition Version 18.1 Release Notes

The *Intel® FPGA SDK for OpenCL™ Standard Edition Release Notes* provides late-breaking information about the Intel Software Development Kit (SDK) for OpenCL[1][2] Standard Edition and the Intel FPGA Runtime Environment (RTE) for OpenCL Standard Edition Version 18.1.

1.1. New Features and Enhancements

The Intel FPGA SDK for OpenCL Standard Edition Version 18.1 and the Intel FPGA RTE for OpenCL Standard Edition Version 18.1 contain no new features or enhancements.

1.2. Operating System Support

Information about OS support for the Intel FPGA SDK for OpenCL Standard Edition is available on the Operating System Support page of the Intel FPGA website.

Related Information

Operating System Support

1.3. Changes to Software Behavior

Items listed in the following table represent cases in which the behaviors of the current release of the Intel FPGA SDK for OpenCL Standard Edition and the Intel FPGA RTE for OpenCL Standard Edition differ from the previous version.

Description	Workaround
N/A	N/A

Items listed in the following table represent cases in which the behaviors of the current release of the Intel FPGA SDK for OpenCL Custom Platform Toolkit and Reference Platforms differ from the previous version.

Description	Workaround
N/A	N/A

(1) OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission of the Khronos Group™.

(2) The Intel FPGA SDK for OpenCL is based on a published Khronos Specification, and has passed the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.

1.4. Known Issues and Workarounds

This section provides information about known issues that affect the Intel FPGA SDK for OpenCL Standard Edition and the Intel FPGA RTE for OpenCL Standard Edition Version 18.1.

Description	Workaround
OpenCL kernels with names longer than 61 characters might fail in the Quartus compiler with an error similar to the following error: `Error (16045): Instance "...|<long_kernel_name>_cra_slave_inst" instantiates undefined entity "<long_kernel_name>_function_cra_slave" File: <filename> Line: <linenumber>`	Reduce the size of the OpenCL kernel name.
Valid OpenCL kernel pipes cannot be passed as arguments in some cases. The symptom is the runtime will receive a `CL_INVALID_BUFFER_SIZE (-61)` error when you enqueue your kernel.	Modify your design to use channels instead of pipes.
The emulator runtime results in an assertion error if a kernel is enqueued 16,000 times.	Do not enqueue a kernel more than 16,000 times.
OpenCL design kernel source files cannot be named `kernel.cl`.	Rename your kernel source file.
When alternatively using subbuffers and their parent buffers, changes written to one might not be reflected in the other.	Unmapping and mapping a buffer forces the subbuffers and their parent buffers to be synced. Unmapping and mapping a buffer between buffer uses should prevent this issue.
The OpenCL Profiler does not support kernels with multiple channel call sites. If you try to use the Profiler on such a kernel, you get the following compilation error: `******* Error: Assert failure at Pass_InsertProfilerHardware.cpp(274) ******* extsig_list.end() != it && (*it)->has_interface_spec() FAILED`	Avoid using the OpenCL Profiler on a kernel that contains multiple channel call sites.

The Intel FPGA SDK for OpenCL Offline Compiler errors out if you pass a struct to a function, as shown in the following example:
`1: struct S{`
`2:  float x;`
`3: };`
`4:`
`5: static inline float get_2x(struct S s){`
`6:  return s.x*2.0f;`
`7: }`
`8:`
`9: kernel void be_useful(`
`10:  global struct s * restrict p,`
`11:  global float * restrict out){`
`12:  *out = get_x(*p);`
`13: }`
	Pass the constituent elements of the struct to the function, as shown in the following example:
	`1: struct S{`
	`2:  float x;`
	`3: };`
	`4:`
	`5: static inline float get_2x(float x){`
	`6:  return x*2.0f;`
	`7: }`
	`8:`
	`9: kernel void be_useful(`
	`10:  global struct S * restrict p,`
	`11:  global float * restrict out){`
	`12:  *out = get_x(p->x);`
	`13: }`

After you set up the Installable Client Driver (ICD) and the FPGA Client Driver (FCD) on an Intel SoC Custom or Reference Platform, the Intel FPGA SDK for OpenCL `aocl link-config` and `aocl linkflags` utilities do not return the correct library paths.	To obtain the correct information on libraries and paths, concatenate the results returned by the `aocl ldflags` and `aocl ldlibs` utilities.
In the OpenCL runtime, making more than one OpenCL context in a multithreaded environment might cause a segmentation fault.	—

This section provides information about known issues that affect the current release of the Intel FPGA SDK for OpenCL Standard Edition Custom Platform Toolkit and Reference Platforms. These issues might also affect Custom Platforms you create for use with the Intel FPGA SDK for OpenCL Standard Edition.

Description	Workaround
Race conditions can occur between enqueue and dequeue buffer operations and host pipe operations. These conditions can results in incorrect data being read or written.	Manually make sure that no enqueue or dequeue buffer operations occur in parallel with host pipe API calls. A way to ensure that buffer operations to do not occur in parallel with host pipe API calls is to do buffer operations as blocking calls before the first host pipe operation and after you are certain that the last host pipe operation has been completed (for example, all the data is read back).

For additional known issue information for the current Intel FPGA SDK for OpenCL version, refer to the Knowledge Base web page.
Additional Known Software Issues Affecting the Intel FPGA SDK for OpenCL Version 18.1

Latest Known Intel FPGA SDK for OpenCL Software Issues

You can find known issue information for previous Intel FPGA SDK for OpenCL versions on the Knowledge Base web page.

Related Information

Knowledge Base

1.5. Software Issues Resolved

The following issues were corrected or otherwise resolved in the Intel FPGA SDK for OpenCL Standard Edition and the Intel FPGA RTE for OpenCL Standard Edition .

Table 1. Issues Resolved in the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL

Customer Service Request Numbers						
11332051	11346929	11363755	11386675	11386675	11408173	11411327
11414858						

1.6. Software Patches Included in this Release

Table 2. Software Patches Included in the Intel FPGA SDK for OpenCL

Software Version	Patch	Customer Service Request Number
Intel FPGA SDK for OpenCL version 18.0	0.28cl	11386675

1.7. Document Revision History of the Intel FPGA SDK for OpenCL Standard Edition Release Notes

Document Version	Intel Quartus® Prime Version	Changes
2018.09.24	18.1	Initial release.