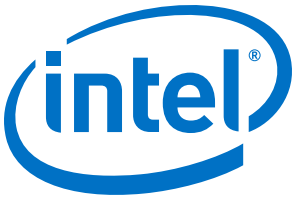

External Memory Interfaces Intel® Agilex™ FPGA IP Core Release Notes

Updated for Intel® Quartus® Prime Design Suite: **19.4**

IP Version: **2.0.0**

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Contents

1. External Memory Interfaces Intel Agilex FPGA IP Core Release Notes

1.1. External Memory Interfaces Intel Agilex FPGA IP v2.0.0

Table 1. v2.0.0 2019.12.16

Description	Impact
Verified in the Intel® Quartus® Prime software v19.4.	Provides external memory interface IP for DDR4 external memory for Intel Agilex™ devices. The tables that follow summarize speed and feature support.

Table 2. Agilex Fabric EMIF IP Speed Support Summary

Protocol	Category	Subcategory	Max Rate (Mbps/MHz)			Support Detail	-1				-2				-3			
			-1	-2	-3		S	C	T	H	S	C	T	H	S	C	T	H
DDR4	Memory Format	UDIMM	3200/1600 (1R)	2666/1333 (1R)	2400/1200 (1R)						X	X	X	up to 1200 MHz	X	X	X	X
			2666/1333 (2R)	2400/1200 (2R)	2133/1067 (2R)						X	X	X		X	X	X	
			2666/1333 (R+R)	2400/1200 (R+R)	2133/1067 (R+R)													
			2133/1067 (2R+2R)	1866/933 (2R+2R)	1600/800 (2R+2R)													
		RDIMM	3200/1600 (1R)	2666/1333 (1R)	2400/1200 (1R)	non-3DS					X	X	X	up to 1200 MHz	X	X	X	X
			2666/1333 (2R)	2400/1200 (2R)	2133/1067 (2R)	non-3DS					X	X	X		X	X	X	
			2666/1333 (R+R)	2400/1200 (R+R)	2133/1067 (R+R)	non-3DS					X	X	X		X	X	X	
			2133/1067 (2R+2R)	1866/933 (2R+2R)	1600/800 (2R+2R)	non-3DS												
			2400/1200 (4R)	2133/1067 (4R)	1866/933 (4R)	non-3DS												
			2666/1333 (2R)	2400/1200 (2R)	2133/1067 (2R)	3DS(2H & 4H)												
			2133/1067 (2R+2R)	1866/933 (2R+2R)	1600/800 (2R+2R)	3DS(2H & 4H)												
		Component	3200/1600 (1R)	2666/1333 (1R)	2400/1200 (1R)	x8,x4,x16,3 DS, 1R Clamshell, 1R Twin-Die x16					X	X	X	up to 1200 MHz	X	X	X	X

continued...

			Max Rate (Mbps/MHz)				-1				-2				-3			
Protocol	**Category**	**Subcategory**	**-1**	**-2**	**-3**	**Support Detail**	**S**	**C**	**T**	**H**	**S**	**C**	**T**	**H**	**S**	**C**	**T**	**H**
			2666/1333 (2R)	2666/1333 (2R)	2400/1200 (2R)	x8, x4, x16												
			2666/1333 (2R)	2400/1200 (2R)	1866/933 (2R)	Clamshell 2R												

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support
- X = supported feature.
- An empty table cell indicates that the feature is not currently supported.

Table 3. Agilex HPS EMIF IP Speed Support Summary

			Max Rate (Mbps/MHz)				-1				-2				-3			
Protocol	Category	Subcategory	-1	-2	-3	Support Detail	S	C	T	H	S	C	T	H	S	C	T	H
DDR4	Memory Format	UDIMM	3200/1600 (1R)	2666/1333 (1R)	2400/1200 (1R)						X	X	X	up to 1200 MHz	X	X	X	X
			2666/1333 (2R)	2400/1200 (2R)	2133/1067 (2R)						X	X	X		X	X	X	
			2666/1333 (R+R)	2400/1200 (R+R)	2133/1067 (R+R)													
			2133/1067 (2R+2R)	1866/933 (2R+2R)	1600/800 (2R+2R)													
		SODIMM	3200/1600 (1R)	2666/1333 (1R)	2400/1200 (1R)						X	X	X	X	X	X	X	X
		RDIMM	3200/1600 (1R)	2666/1333 (1R)	2400/1200 (1R)	non-3DS					X	X	X	up to 1200 MHz	X	X	X	X
			2666/1333 (2R)	2400/1200 (2R)	2133/1067 (2R)	non-3DS					X	X	X		X	X	X	
			2666/1333 (R+R)	2400/1200 (R+R)	2133/1067 (R+R)	non-3DS					X	X	X		X	X	X	
			2133/1067 (2R+2R)	1866/933 (2R+2R)	1600/800 (2R+2R)	non-3DS												
			2400/1200 (4R)	2133/1067 (4R)	1866/933 (4R)	non-3DS												
			2666/1333 (2R)	2400/1200 (2R)	2133/1067 (2R)	3DS(2H & 4H)												
			2133/1067 (2R+2R)	1866/933 (2R+2R)	1600/800 (2R+2R)	3DS(2H & 4H)												
		Component	3200/1600 (1R)	2666/1333 (1R)	2400/1200 (1R)	x8,x4,x16,3 DS, 1R Clamshell, 1R Twin-Die x16					X	X	X	up to 1200 MHz	X	X	X	X

continued...

			Max Rate (Mbps/MHz)				-1				-2				-3			
Protocol	**Category**	**Subcategory**	**-1**	**-2**	**-3**	**Support Detail**	**S**	**C**	**T**	**H**	**S**	**C**	**T**	**H**	**S**	**C**	**T**	**H**
			2666/1333 (2R)	2666/1333 (2R)	2400/1200 (2R)	x8, x4, x16												
			2666/1333 (2R)	2400/1200 (2R)	1866/933 (2R)	Clamshell 2R												

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support
- X = supported feature.
- An empty table cell indicates that the feature is not currently supported.

Table 4. Agilex EMIF IP Feature Support Summary

Protocol	Category	Subcategory	Supported?	S	C	T	H
DDR4	Interface Width	<=72 with DIMM	X	X	X	X	X
		<= 72 Component	X	X	X	X	X
	Controller	Hard Controller	X	X	X	X	X
	PHY	Hard PHY	X	X	X	X	X
	3DS	3DS	X (1D2R/ 1D2R only)	X	X	X	
	Design example		X	X	X	X	X
	Rate (core)	Quarter Rate	X	X	X	X	X
	DBI	Read DBI	X	X	X	X	X
		Write DBI	X	X	X	X	X
	Mirroring	Address mirroring for odd ranks for multi ranks DIMM	X	X	X	X	X
	DM	DM Pins	X	X	X	X	X
	Preamble	Read Preamble Settings	X	X	X	X	X
		Write Preamble Settings	X	X	X	X	X
	Refresh[1]	Temperature Controlled Refresh					
		Fine Granularity Refresh					
		Auto Self-refresh Method					
		Self-refresh					
	ODT[1]	Input Buffer During Power-down Mode					
	Controller	ECC	X	X	X	X	X
		Reordering	X	X	X	X	X
		Auto Power-down	X	X	X	X	
		User Refresh					

continued...

Protocol	Category	Subcategory	Supported?	S	C	T	H
		Auto Precharge		X	X	X	
		Command Priority					
	Calibration	Address/ Command Calibration	X	X	X	X	X
		Multi-rank Calibration	X	X	X	X	X
	Debug	EMIF Toolkit	X		X	X	X

Note[1]: Feature not validated in hardware.

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

- X = supported feature.
- An empty table cell indicates that the feature is not currently supported.

Table 5. Agilex EMIF HPS IP Feature Support Summary

Protocol	Category	Subcategory	Supported?	S	C	T	H
DDR4	Interface Width	<=72 with DIMM	X		X	X	X
		<= 72 Component	X		X	X	X
	Controller	Hard Controller	X		X	X	X
	PHY	Hard PHY	X		X	X	X
		PHY only					
	Rate (core)	Quarter Rate	X		X	X	X
		Half Rate	X		X	X	X
	DM	DM Pins[1]	X		X	X	X
	Preamble	Read Preamble Settings	X		X	X	X
		Write Preamble Settings	X		X	X	X
	Refresh[2]	Temperature Controlled Refresh					
		Fine Granularity Refresh					

continued...

Protocol	Category	Subcategory	Supported?	S	C	T	H
		Auto Self-refresh Method					
		Self-refresh About					
	ODT[2]	Input Buffer During Power-down Mode					
	Controller	ECC			X	X	X
		Reordering	X		X	X	X
		Auto Power-down	X		X	X	
		User Refresh					
		Command Priority					
	Calibration	Address/ Command Calibration	X		X	X	X
	Debug	EMIF Toolkit					

- Note[1]: HPS EMIF always requires DM pins.
- Note[2]: Feature not validated in hardware.

Support level key:
- S = simulation support
- C = compilation support
- T = timing support
- H = hardware support

- X = supported feature.
- An empty table cell indicates that the feature is not currently supported.

Table 6. Agilex EMIF IP Debug Support Summary

Category	Subcategory		Supported?
Debug Support	On-chip Debug	On-chip Debug with Soft Nios®	
	EMIF Toolkit	Calibration Margin	X
		Rerun Calibration	X
		Vref Margining	
		Driver Margining	X
		Efficiency Monitor	
		ODT Calibration	X
		Multi-interface Support	X

- X = supported feature.
- An empty table cell indicates that the feature is not currently supported.