Arria V Hard IP for PCI Express IP Core Release Notes

2016.10.31

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If a release note is not available for a specific IP core version, the IP core has no changes in that version.

Arria V Hard IP for PCI Express IP Core v16.1

Table 1: v16.1 October 2016

Description	Impact
For the Avalon-MM with DMA interface, increased the maximum DMA transfer size to 1 megabyte (MB) for both the 128- and 256-bit interfaces.	Reduces the number of descriptors required to transfer data.

Related Information

- **Arria V Avalon-ST Interface for PCIe Solutions User Guide**
  For the Avalon-ST Interface to the Application. Layer
- **V-Series Avalon-MM DMA Interface for PCIe Solutions User Guide**
  For the Avalon-MM interface and DMA. functionality
- **Arria V Avalon-MM Interface for PCIe Solutions User Guide**
  For the Avalon-MM interface with no DMA.
- **Errata for the Arria V Hard IP for PCI Express IP Core in the Knowledge Base**
- **Introduction to FPGA IP Cores**
  Provides general information about all FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- **Creating Version-Independent IP and Qsys Simulation Scripts**
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- **Project Management Best Practices**
  Guidelines for efficient management and portability of your project and IP files.

Arria V Hard IP for PCI Express IP Core v16.0

Table 2: v16.0 May 2016

Description	Impact
For the V-Series Avalon® Memory-Mapped (Avalon-MM) DMA for PCI Express IP Core, rearchitected the Write DMA module for the 128-bit interface to the Application Layer.	Provides higher throughput for external memories.
For the V-Series Avalon-MM DMA for PCI Express IP Core, the 256-bit interface to the Application Layer now supports a maximum transfer size of 64 kilobytes (KB).	Large transfers require fewer descriptor table entries.

Arria V Hard IP for PCI Express IP Core v15.0

Table 3: v15.0 May 2015

Description	Impact
In IP core variations with the Avalon-MM DMA interface, added support for downstream burst read request for a payload of size up to 4 KBytes, if **Enable burst capability for RXM BAR2 port** is turned on in the Parameter Editor. Previous maximum downstream read request payload size was 512 bytes.	If you choose the Avalon-MM DMA interface, the IP core can receive and process a burst read request for a payload of any size supported by the PCI Express specification (up to 4 KBytes), if it receives such a burst read request on the PCI Express link.
In IP core variations with the Avalon-MM interface, added support to send message TLPs with data payload of any length from a Root Port.	If you choose the Avalon-MM interface, a Root Port IP core can send messages with payload greater than 1 dword.

Arria V Hard IP for PCI Express IP Core v14.1

Table 4: v14.1 December 2014

Description	Impact
Reduced Quartus II compilation warnings by 50%.	Reduces time required to vet compilation warnings.

Arria V Hard IP for PCI Express IP Core v14.0

Table 5: v14.0 June 2014

Description	Impact
Upgraded the Avalon-ST version to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Upgraded Arria V Hard IP for PCI Express IP core to support the new IP Catalog.	-
Added support for new, V-Series PCIe with Avalon-MM DMA Interface IP Core.	-
Arria V Avalon-MM Hard IP for PCI Express IP core. : • Added access to selected Configuration Space and link status registers through the optional Control Register Access (CRA) Avalon-MM slave port. • Added optional hard IP status bus that includes signals necessary to connect the Transceiver Reconfiguration Controller IP Core. • Added optional hard IP status extension bus which includes signals that are useful for debugging, including: link training, status, error, and Configuration Space signals.	All of these new features are optional. If you include either the hard IP status bus or status extension bus in you design, you must regenerate your design and connect the new bus

Arria V Hard IP for PCI Express IP Core v13.1

Table 6: v13.1 November 2013

Description	Impact
Added support for Gen2 Configuration via Protocol (CvP) using an **.ini** file. Contact your sales representative for more information.	-