External Memory Interfaces Intel® Arria® 10 FPGA IP Core Release Notes

2019.07.01

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If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Intel Quartus Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel® Quartus® Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP versioning scheme (X.Y.Z) number changes from one software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

Intel Quartus Prime Design Suite Update Release Notes

External Memory Interfaces Intel Arria® 10 FPGA IP Core v19.1.0

Table 1: v19.1.0 2019.07.01

Intel Quartus Prime Version	Description	Impact
19.2	Verified in the Intel Quartus Prime software v19.2.	—

External Memory Interfaces Intel Arria® 10 FPGA IP 19.1

Table 2: v19.1 April 2019

Description	Impact
Verified in the Intel Quartus Prime software v19.1.	—

Related Information

- **External Memory Interfaces Intel Arria 10 FPGA IP User Guide**

- External Memory Interfaces Intel Arria 10 FPGA IP Design Example User Guide
- Intel Quartus Prime Design Suite Release Notes
- Errata for Intel Arria 10 External Memory Interface IP in the Knowledge Base

External Memory Interfaces Intel Arria® 10 FPGA IP 18.1

Table 3: v18.1 September 2018

Description	Impact
Verified in the Intel Quartus Prime software v18.1.	Provides external memory interface IP for DDR3, DDR4, QDR II/II+/Xtreme, QDR-IV, RLDRAM3, and LPDDR3 protocols for Intel Arria® 10 devices.

Related Information

- External Memory Interfaces Intel Arria 10 FPGA IP User Guide
- External Memory Interfaces Intel Arria 10 FPGA IP Design Example User Guide
- Intel Quartus Prime Design Suite Release Notes
- Errata for Intel Arria 10 External Memory Interface IP in the Knowledge Base

External Memory Interfaces Intel Arria 10 FPGA IP 18.0

Table 4: v18.0 May 2018

Description	Impact
Verified in the Intel Quartus Prime software v18.0.	Provides external memory interface IP for DDR3, DDR4, QDR II/II+/Xtreme, QDR-IV, RLDRAM3, and LPDDR3 protocols for Intel Arria 10 devices.

Related Information

- External Memory Interfaces Intel Arria 10 FPGA IP User Guide
- External Memory Interfaces Intel Arria 10 FPGA IP Design Example User Guide
- Intel Quartus Prime Design Suite Release Notes
- Errata for Intel Arria 10 External Memory Interface IP in the Knowledge Base

Intel Arria 10 External Memory Interface IP 17.1

Table 5: v17.1 November 2017

Description	Impact
Verified in the Intel Quartus Prime software v17.1.	—

Related Information

- Intel Arria 10 External Memory Interfaces IP User Guide
- Intel Arria 10 External Memory Interfaces IP Design Example User Guide
- Intel Quartus Prime Design Suite Release Notes
- Errata for Intel Arria 10 External Memory Interface IP in the Knowledge Base

Arria 10 External Memory Interface IP 17.0

Table 6: v17.0 May 2017

Description	Impact
Verified in the Quartus Prime software v17.0	—

Related Information

- External Memory Interface Handbook
- Errata for Arria 10 External Memory Interface IP in the Knowledge Base

Arria 10 External Memory Interface IP 16.1

Table 7: v16.1 November 2016

Description	Impact
Implemented fix to address hardware calibration problems with DDR4 LRDIMM interfaces. (This change is a final bit-settings change for 10AX115 devices.)	To incorporate this fix in existing DDR4 LRDIMM designs, regenerate the DDR4 IP and recompile the design.
Modified parameter editor for DDR4 RDIMM and LRDIMM to accept individual RDIMM/LRDIMM SPD data directly, without manual encoding. The IP then calculates the encoded RCD and DB configuration settings.	If you are upgrading from a previous version that uses the encoded values, those values are still accepted by the new version of the IP.

Description	Impact
DDR3 LRDIMM usage is currently restricted. If you select LRDIMM, you will not be able to generate an external memory interface IP for DDR3.	Cannot generate EMIF IP for DDR3 LRDIMM. Contact Intel for support.

Related Information

- **External Memory Interface Handbook**
- **Errata for Arria 10 External Memory Interface IP in the Knowledge Base**