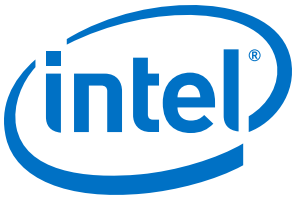

50G Interlaken IP Core Release Notes

RN-1105
2016.05.02

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Contents

1 50G Interlaken IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Intel Quartus Prime Design Suite Update Release Notes*.

Related Links

Intel Quartus Prime Design Suite Update Release Notes

1.1 50G Interlaken IP Core v16.0

Table 1. Version 16.0 May 2016

Description	Impact	Notes
Added **Example Designs** tab that automatically generates both simulation and hardware example designs with the parameters you specify.	You can now download an example design to the Altera Arria 10 GX FPGA Development Kit using only the automatically generated files.	

Related Links

- 50G Interlaken MegaCore Function User Guide
- Errata for 50G Interlaken IP core in the Knowledge Base

1.2 50G Interlaken IP Core v15.1

Table 2. Version 15.1 November 2015

Description	Impact	Notes
Added new **Enable Native XCVR PHY ADME** parameter for Arria 10 variations..	Upgrading the IP core to incorporate this feature is optional. This change does not affect the top-level signals of the IP core.	This parameter exposes control of transceiver configuration features.
Added hardware design example for Arria 10 variations.	A hardware design example is now available with Arria 10 variations of the 50G Interlaken IP core.	
Modified instructions to generate legacy testbench.		

Related Links

- 50G Interlaken MegaCore Function User Guide
- Errata for 50G Interlaken IP core in the Knowledge Base

1.3 50G Interlaken IP Core v15.0

Table 3. Version 15.0 May 2015

Description	Impact	Notes
Added new **TX scrambler seed** parameter.	This feature adds support for modification of the TX scrambler seed for Arria 10 variations. If your design includes multiple IP cores, you should ensure they have different TX scrambler seed values. Previously this functionality was not available for Arria 10 variations. In addition, starting in the IP core version 15.0, you must refrain from modifying the RTL parameter SCRAM_CONST in Stratix V and Arria V GZ variations, and use the new parameter in the Parameter Editor instead.	

Related Links

- 50G Interlaken MegaCore Function User Guide
- Errata for 50G Interlaken IP core in the Knowledge Base

1.4 50G Interlaken IP Core v14.1

Table 4. Version 14.1 December 2014

Description	Impact	Notes
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	IYou must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	

Related Links

- 50G Interlaken MegaCore Function User Guide
- Errata for 50G Interlaken IP core in the Knowledge Base

1.5 50G Interlaken IP Core v14.0 Arria 10 Edition

Table 5. Version 14.0 Arria 10 Edition August 2014

Description	Impact	Notes
Verified in the Quartus II software v14.0 Arria 10 Edition.		

Related Links

- 50G Interlaken MegaCore Function User Guide
- Errata for 50G Interlaken IP core in the Knowledge Base

1.6 50G Interlaken IP Core v14.0

Table 6. Version 14.0 June 2014

Description	Impact	Notes
New required frequency for input clock signals `tx_usr_clk` and `rx_usr_clk` is 250 MHz, and the two clocks must be driven at the same frequency. If you provide a clock with a different frequency, it must be in the range of 200 MHz to 300 MHz, and you must modify the new hidden (RTL) parameter TX_USR_CLK_MHZ to the new value in the files `<instance_name>/ilk_core_50g.sv` for synthesis and `<instance_name>_sim/ilk_core_50g.sv` for simulation.		
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.		
Improved resource utilization by 20% and latency by 55%.		

Related Links

- Introduction to Altera IP Cores
- 50G Interlaken MegaCore Function User Guide
- Errata for 50G Interlaken IP core in the Knowledge Base

1.7 50G Interlaken IP Core v13.1 Arria 10 Edition

Table 7. Version 13.1 Arria 10 Edition December 2013

Description	Impact	Notes
Added support for Arria 10 devices. IP core variations that target an Arria 10 device have additional interfaces and design requirements.		

Table 8. 50G Interlaken IP Core Signal Changes

Signals added or modified in version 13.1 Arria 10 Edition.

Old Signal Name	New Signal Name	Notes
—	tx_serial_clk	New interface to external TX PLL. Relevant for Arria 10 variations only.
—	tx_pll_locked	
—	tx_pll_powerdown	
—	tx_cal_busy	
—	reconfig_clk	New Arria 10 transceiver reconfiguration interface. Relevant for Arria 10 variations only.
—	reconfig_reset	
—	reconfig_read	
—	reconfig_write	
—	reconfig_address[12:0]	
—	reconfig_readdata[31:0]	
—	reconfig_waitrequest	
—	reconfig_writedata[31:0]	
reconfig_to_xcvr	Not present in Arria 10 variations.	Transceiver reconfiguration interface for Arria V and Stratix V variations. This interface is present only in Arria V and Stratix V variations (as

continued...

Old Signal Name	New Signal Name	Notes
reconfig_from_xcvr	Not present in Arria 10 variations.	supported in past and future versions of the Quartus II software). It is not present in Arria 10 variations.

Related Links

- 50G Interlaken MegaCore Function User Guide
- Errata for 50G Interlaken IP core in the Knowledge Base

1.8 50G Interlaken IP Core v13.1

Table 9. Version 13.1 November 2013

Description	Impact	Notes
Verified in the Quartus II software v13.1.		

Related Links

- 50G Interlaken MegaCore Function User Guide
- Errata for 50G Interlaken IP core in the Knowledge Base

1.9 50G Interlaken IP Core v13.0

Table 10. Version 13.0 May 2013

Description	Impact	Notes
Initial release.		

Related Links

- 50G Interlaken MegaCore Function User Guide
- Errata for 50G Interlaken IP core in the Knowledge Base