

40- and 100-Gbps Ethernet MAC and PHY IP Core Release Notes

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If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Altera Complete Design Suite Update Release Notes*.

Related Information

[Altera Complete Design Suite Update Release Notes](#)

40- and 100-Gbps Ethernet MAC and PHY IP Core v14.1

Table 1: Version 14.1 December 2014

| Description | Impact | Notes |
|---|--------|-------|
| Verified in the Quartus II software v14.1 | | |

Related Information

- [40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide](#)
- [Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base](#)

40- and 100-Gbps Ethernet MAC and PHY IP Core v14.0 Update 2

Table 2: Version 14.0 Update 2 September 2014

| Description | Impact | Notes |
|--|--|-------|
| Fixed an issue in which incoming runt Ethernet packets of size one byte to eight bytes caused the 40GbE IP core to hang instead of handling the error. | If you upgrade to version 14.0 Update 2 of the Quartus II software, you must upgrade your 40-100GbE IP core to incorporate this fix. The fix has no effect on 100GbE IP cores, which did not have the issue. However, the previous versions of the 40-100GbE IP core require upgrade with the Quartus II software. | |

Related Information

- [40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide](#)
- [Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base](#)

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40- and 100-Gbps Ethernet MAC and PHY IP Core v14.0

Table 3: Version 14.0 June 2014

| Description | Impact | Notes |
|--|---|-------|
| Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to <i>IP Catalog and Parameter Editor</i> in <i>Introduction to Altera IP Cores</i> . | Upgrading your IP core for this change is optional. | |
| Added OpenCore Plus support for 40GBASE-KR4 variations. | Upgrading your IP core for this change is optional. | |

Related Information

- [Introduction to Altera IP Cores](#)
- [40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide](#)
- [Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base](#)

40- and 100-Gbps Ethernet MAC and PHY IP Core v13.1

Table 4: Version 13.1 November 2013

| Description | Impact | Notes |
|--|--------|-------|
| Added 40GBASE-KR4 option with FEC and with auto-negotiation and link training mode options. | | |
| Added Synchronous Ethernet clock support option in Stratix V devices. The option separates the TX PLL and RX CDR input reference clocks (<code>tx_ref_clk</code> and <code>rx_ref_clk</code> signals replace <code>ref_clk</code> for these variations) and exposes the RX recovered clock. | | |
| Exposed link fault signals <code>remote_fault_status</code> and <code>local_fault_status</code> in duplex variations. | | |
| Exposed PHY status signals <code>tx_lanes_stable</code> and <code>lanes_deskewed</code> in MAC&PHY variations. | | |
| Updated and simplified the example design and testbench. The testbench stimulus is simpler and the user no longer needs to configure the DUT with a specific name and clock rate. | | |

Related Information

- [40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide](#)
- [Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base](#)

40- and 100-Gbps Ethernet MAC and PHY IP Core v13.0

Table 5: Version 13.0 May 2013

| Description | Impact | Notes |
|---|--------|-------|
| Added preamble pass-through option. | | |
| Added transmitter average inter-packet gap (IPG) adjustment option. | | |

Related Information

- [40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide](#)
- [Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base](#)

40- and 100-Gbps Ethernet MAC and PHY IP Core v12.1

Table 6: Version 12.1 November 2012

| Description | Impact | Notes |
|--|--------|-------|
| Verified with the Quartus II software v12.1. | | |

Related Information

- [40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide](#)
- [Errata for 40- and 100-Gbps Ethernet MAC and PHY IP core in the Knowledge Base](#)