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1. E-tile Dynamic Reconfiguration Design Example Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the Intel® Quartus® Prime Design Suite Update Release Notes.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP versioning scheme (X.Y.Z) number changes from one software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information
- Intel Quartus Prime Design Suite Update Release Notes
- E-tile Hard IP for Ethernet and CPRI PHY Intel FPGA IPs User Guide
- E-tile Hard IP Intel Stratix® 10 Design Examples User Guide: Ethernet, CPRI PHY, and Dynamic Reconfiguration
- Errata for Intel FPGA IPs in the Knowledge Base

1.1. E-tile Dynamic Reconfiguration Design Example v19.3.0

Table 1. v19.3.0 2019.09.30

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<th>Intel Quartus Prime Version</th>
<th>Description</th>
<th>Impact</th>
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<tr>
<td>19.3</td>
<td>Initial release for Intel Agilex™ devices. • Added support for the following dynamic reconfiguration design examples: — 10G/25G Ethernet (single-channel design only) — 25G Ethernet to CPRI</td>
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*Other names and brands may be claimed as the property of others.
**1.2. E-tile Dynamic Reconfiguration Design Example v19.2.0**

Table 2. v19.2.0 2019.07.01

<table>
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<tr>
<th>Intel Quartus Prime Version</th>
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<th>Impact</th>
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| 19.2                        | • Added new 25G Ethernet to CPRI Protocol dynamic reconfiguration protocol design  
                              • Added new 25G Ethernet to CPRI dynamic reconfiguration design example | — |

**1.3. E-tile Dynamic Reconfiguration Design Example v19.1**

Table 3. v19.1 April 2019

<table>
<thead>
<tr>
<th>Description</th>
<th>Impact</th>
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| Initial release for Intel Stratix® 10 devices.  
  • Added support for the following dynamic reconfiguration design examples:  
    — 10G/25G Ethernet (single-channel design only)  
    — 10G/24G CPRI (single-channel design only) | — |

**1.4. E-tile Dynamic Reconfiguration Design Example User Guide Archives**

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

If an IP core version is not listed, the user guide for the previous IP core version applies.

<table>
<thead>
<tr>
<th>IP Core Version</th>
<th>Intel Stratix 10 User Guide</th>
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<tr>
<td>19.2</td>
<td>E-tile Hard IP Intel Stratix 10 Design Examples User Guide</td>
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<td>E-tile Hard IP Intel Stratix 10 Design Examples User Guide</td>
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<td>18.1.1</td>
<td>E-tile Hard IP for Ethernet Intel Stratix 10 FPGA IP Design Example User Guide</td>
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