



Embedded Memory (RAM: 1-PORT, RAM: 2-PORT, RAM: 4-PORT, ROM: 1- PORT, and ROM: 2-PORT) Intel FPGA IP Release Notes



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If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Intel Quartus Prime Design Suite Update Release Notes*.

Related Information

[Intel Quartus Prime Design Suite Update Release Notes](#)

Embedded Memory (RAM: 1-PORT, RAM: 2-PORT, RAM: 4-PORT, ROM: 1-PORT, and ROM: 2-PORT) Intel® FPGA IP v18.0

Table 1. v18.0 May 2018

Description	Impact
Renamed the following IP cores as per Intel rebranding: <ul style="list-style-type: none"> • RAM: 1-PORT IP core to RAM: 1-PORT Intel® FPGA IP • RAM: 2-PORT IP core to RAM: 2-PORT Intel FPGA IP • RAM: 4-PORT IP core to RAM: 4-PORT Intel FPGA IP • ROM: 1-PORT IP core to ROM: 1-PORT Intel FPGA IP • ROM: 2-PORT IP core to ROM: 2-PORT Intel FPGA IP 	—

Related Information

- [Introduction to Intel FPGA IP Cores](#)
- [Intel Stratix® 10 Embedded Memory User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)