Cyclone V SoC HPS Release Notes

2014.09.19

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These release notes cover v. 13.0 through v. 14.0.1 of the Altera® Cyclone® V system on a chip (SoC) hard processor system (HPS).

These release notes describe the following topics:

- Features supported by the Cyclone V SoC HPS
- Intellectual property (IP) for the Cyclone V SoC HPS, including the Cyclone V SoC HPS component
- Embedded software for the Cyclone V SoC HPS
- Known issues and Errata

Related Information

Quartus II Software and Device Support Release Notes Version 14.0

Product Revision History

Table 1: SoC HPS Revision History

Version	Date	Description
14.0.1	September 2014	• Includes Development Studio 5 Altera Edition version 5.19.1. • SoC EDS now supports Angstrom and LTSI 3.10. • GHRD build is now based on ACDS 14.0.1. Improvements to the Device Tree Generator: • `sopc2dts` no longer generates incorrect USB node for newer device driver. • Fixed the issue with the dangling reference to a non-existent clock so that the DTG successfully compiles. Improvements to the Hardware LIBs: • Changes to the new tool chains such as compiler, linker, and loader. • Added the capability to support memory sizes larger than 32 GB when setting the bus width in a 64 GB Micro SD card. • Fixed the compilation failure when using Altera-SoCFPGA-Hardwar-eLib-FPGA-CV-GNU. • Added functionality for the SD/MMC to flush and invalidate the buffers and descriptors for the SD card DMA.

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Version	Date	Description

		• Fixed the issue that did not allow SD write in non DMA mode.
		• Fixed the Input and Output ID error in alt_address_space.c.
		• Improvements to the SD/MMC.
		  • New features.
		  • Added `dprintf` on failure code paths.
		  • Enabled SDSC/SDXC support with access up to 4GB.
		  • Enabled query of capacity, high speed and supported bus widths.
		  • Simplified API to set SD/MMC clock.
		  • Enable high-speed 50 MHz support.
		  • Bug fixes.
		  • Increased SD/MMC speed setting.
		  • Corrected definition of FIFO full status to prevent writes in non-DMA mode failing.
		  • SD/MMC no longer fails if DMA is enbaled before enumeration.
		  • Build no longer breaks in `dprintf` with armcc compiler.
		  • `smplsel` and `devsel` are set to non-zero when `use_hold_reg` is set per the IP's datasheet.
		  • Removed response query code on commands that do not send a response.
		  • Fixed the issue of receiving a failure when accessing some SanDisk cards.
		• Fixed various HWLIB issues that pertain to various IPs, such as QSPI and UART.
		Improvements to the Preloader:
		• Added the DWC2 OTG USB driver to fix the incompatible issue that the default USB driver was having with the Arria V and Cyclone V devices.
		• Fixed the issue where the MAC address registers clear after executing a `ping` command.
		• Fixed clock divider calculation error for bypass mode.
		• Added a workaround for HPS PLL lock issue after power-on reset.

Version	Date	Description
14.0	June 2014	• Includes Development Studio 5 Altera Edition version 5.18. • Improved bare metal flow with GCC. • Improvements to the SoC EDS • Supports a 64-bit install • Added ability to create a bare metal project from scratch. • Added Altera boot disk utility **alt-boot-disk-util.exe**. • Added ability to set clock for preloader generation flow from Qsys. • HPS component upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*. **Note:** 32-bit host systems are no longer supported.

13.1	November 2013	• Cyclone V SoC devices available with full silicon support
		• Improved pin MUX interface in the HPS component parameter editor
		• Improved timings models and customizations in the PowerPlay Early Power Estimator
		• Improvements to the SoC EDS
		  • Supports a 32-bit install
		  • Added Quartus II programmer and drivers
		  • Added FTDi USB-to-UART drivers
		  • DS-5 Altera Edition upgraded to ARM DS-5 v5.15.0
		  • Enhanced SoC Hardware Library support
		  • Upgraded Linux kernel support
		  • Updated reference design
		  • Updated device tree generator
		  • Updated U-boot
		  • New preloader features
		• HPS component verified with the Quartus II software v13.1

13.0 SP1	July 2013	• DS-5 Altera Edition upgraded to ARM DS-5 v5.14.1
		• SoC EDS improvements
		  • Software support added for SDRAM ECC
		  • Device tree generator added to EDS
		  • FPGA-to-SDRAM interface support added to EDS
		  • SoC Hardware Library support for UART, GPIO, DMA, and Int Ctrl
		  • Bug fixes
		• HPS component verified with the Quartus II software v13.0 SP1

Version	Date	Description
13.0	May 2013	• Introduces the SoC HPS Embedded Design Suite (EDS) • HPS component verified with the Quartus II software v13.0 • The 10GBASE-R PHY IP core adds device support for the Cyclone V SoC

Related Information

- **Quartus II Software and Device Support Release Notes**
  For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*
- **FPGA-Adaptive Software Debug and Performance Analysis**
  For more information about what is new in the SoC EDS, refer to the FPGA-Adaptive Software Debug and Performance Analysis document.

What's New in 14.0.1

What's New in the Cyclone V SoC EDS for 14.0.1

The Cyclone V SoC v14.0.1 provides an enhanced out of box experience:

- The SoC EDS Hardware Libs added new APIs and design examples:
  - New APIs:
    - QSPI - to read and write the QSPI flash
    - I^2C - to help use the I^2C serial interface
    - SPI - to read and write the serial SPI interface
    - NAND - to access NAND-based Flash non-volatile memory
    - SD/MMC - for SD/MMC removable Flash media
    - ECC - to help use the Error Correction Code (ECC) hardware (excluding SD/MMC and NAND Flash memory)
    - CAN - to support Controller Area Network (CAN) bus protocol handling and processing
  - New design examples
    - SPI read/write from/to an EEPROM example with armcc compiler: `<Altera-SocFPGA-HardwareLib-SPI-RW-CV-ARMCC>`
    - SPI read/write from/to an EEPROM example with gnu compiler: `<Altera-SocFPGA-HardwareLib-SPI-RW-CV-GNU>`
    - ECC L2 example with armcc compiler: `<Altera-SocFPGA-HardwareLib-ECCl2-CV-ARMCC>`
    - ECC L2 example with gnu compiler: `<Altera-SocFPGA-HardwareLib-ECCl2-CV-GNU>`
    - FPGA example with armcc compiler: `<Altera-SocFPGA-HardwareLib-FPGA-CV-ARMCC>`
    - FPGA example with gnu compiler: `<Altera-SocFPGA-HardwareLib-FPGA-CV-GNU>`

    Note: Each of the above design examples also support semihosted and non-semihosted configurations. You must make the choice in the Makefile.
- Preloader added new design examples - Minimal Preloader (MPL) example: `<Altera-SocFPGA-HardwareLib-MPL-CV-ARMCC>`

  Note: Only ARMCC version is released. Effort for a GNU version release is still to come.

What's New in 14.0

What's New in the Cyclone V SoC EDS for 14.0

The Cyclone V SoC v14.0 provides an enhanced out of box experience:

- DS-5 Altera Edition with ARM DS-5 v5.18.0, including:
  - Improved bare metal flow with GCC
  - Ability to create a bare metal project from scratch
- SoC Hardware Library support including:
  - APIs for I^2C, SPI, ECC, and memory coherence
  - Support for system manager
  - Flash memory interface for NAND, QSPI, and SD/MMC
  - SoC Hardware Library compiler support
  - New example designs to cover every API that can be run stand-alone without semihosting
  - Improved visibility of hardware libraries
- Preloader Features:
  - Improved integration between Qsys and preloader with regards to clocks.
  - Preloader generator tool enhancements for peripheral clock configuration.
  - PLL configuration in preloader generator.
- HPS component upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.

Related Information

- **Quartus II Software and Device Support Release Notes**
  For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*
- **FPGA-Adaptive Software Debug and Performance Analysis**
  For more information about what is new in the SoC EDS, refer to the FPGA-Adaptive Software Debug and Performance Analysis document.

What's New in 13.1

What's New in Cyclone V SoC Silicon Support for v13.1

The Cyclone V SoC device family is fully supported.

What's New in the HPS Component for v13.1

The HPS component parameter editor has been updated to make it easier to create valid pin assignments.

The **Peripheral Pin Multiplexing** tab has been enhanced with the following features:

- MUX values clearly shown in table
- Preview of available pin locations for each peripheral
- Components color-coded in pin table
- Selected pins shown in pin table with bolding and borders
- Faster GPIO and Loaner I/O selection
- Row with pin conflicts shown in red

What's New in the Cyclone V SoC EDS for v13.1

- DS-5 Altera Edition upgraded to ARM DS-5 v5.15.0 -provides the following improvements:
  - Official Gator/Streamline support for SoC Linux 3.9
  - ThreadX and uC/OS III kernel awareness
- Quartus II Standalone Programmer, including USB-Blaster II driver and binaries
- FTDi USB-to-UART drivers used on Cyclone V development boards
- Upgraded SoC Hardware Library support:
  - New APIs: Cache, MMU
  - Validated with ARMCC
- Support for Linux kernel 3.9
  - New drivers for FPGA bridges, DMA, QSPI, and watchdog timers
- Cyclone V GHRD is pre-signal tapped
- Device tree generator support for Linux 3.9
- v2013.01.01 U-Boot Code Base
- New preloader features
  - Performance improvements - SD/MMC now uses DMA to transfer data
  - UART baud rate increased from 57600 to 115200
  - QSPI auto calibration
  - Improvements to bridge reset release management
  - U-boot independent of Quartus-generated preloader handoff

What's New in 13.0 SP1

What's New in the Cyclone V SoC EDS for v13.0 SP1

- DS-5 Altera Edition upgraded to ARM DS-5 v5.14.1—provides the following improvements:
  - Better support for partner boards
  - Usability improvements
  - Bug fixes
  - Better error messages
  - Gator driver upgraded to work with Altera target
- Software support added for SDRAM ECC—single-bit error (SBE) recovery is enabled in the Preloader. For setup and usage information, refer to the SoC Linux Community Portal.
- Device tree generator added—Linux Device Tree generation is enabled for proper initialization of Linux device drivers. Device Tree generation includes the complete flow, from the SOPC Information File (**.sopcinfo**) input to the device tree blob (**.dtb**) file output.
- FPGA-to-SDRAM interface support added—the Preloader is updated to support soft IP access to the HPS SDRAM, through the FPGA-to-SDRAM interface
- SoC Hardware Library supports UART, GPIO, DMA, Int Ctrl

Related Information

- **SoC HPS errata in KB**
- **Rocketboards**

What's New in 13.0

What's New in the Cyclone V SoC EDS for 13.0

The Cyclone V SoC v. 13.0 introduces the Altera system on a chip (SoC) Embedded Design Suite (EDS).

What's New in Arria 10 SoC PowerPlay Support for v13.1

Altera's Web-based PowerPlay Early Power Estimator (EPE) is updated to provide more user customizations and more accurate timing models for the Arria 10 SoC device family. Refer to the PowerPlay EPE for more information.

Related Information

PowerPlay Early Power Estimator

Known Issues and Errata

Table 2: Known Issues and Errata

Version	Date	Description
14.0.1	September 2014	• 181269 - Add Mentor Bare-Metal Tool Support for Altera boards. • 199644 - SoC EDS: Add link to Bare-Metal Compiler Getting Started Guide. • 203309 - The GHRD tgz files contain intermediate files that may not be useful. • 226737 - Linking error occurs because a 32-bit cross-compiler is shipped with the 64-bit version of SoCEDS instead of a 64-bit gcc cross-compiler. • 227197 - Add more documentation on how to run the HelloWorld example designs. • 229396 - When BSEL is set to 0, all regression tests using preloader and then uboot fail in soceds/14.0.1/234 and soceds/14.1/143.

Document Revision History

Date	Changes
September 2014	Updated for v14.0.1
July 2014	Updated for v14.0
November 2013	Updated for v13.1
June 2013	Updated for v13.0 SP1
December 2012	Initial publication, v12.1