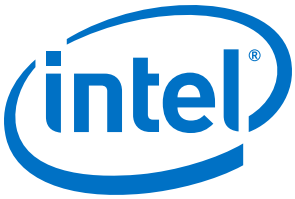

Intel® SoC FPGA Embedded Development Suite (SoC EDS) Release Notes

Updated for Intel® Quartus® Prime Design Suite: **19.1**

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Intel® SoC FPGA Embedded Development Suite (SoC EDS) Intel® Quartus® Prime version 19.1 Release Notes

The Intel® SoC FPGA Embedded Development Suite (SoC EDS) version 19.1 release notes provide information about the 18.1 through 19.1 software release versions for the SoC EDS Professional Edition of the Intel SoC FPGA Embedded Development Suite (SoC EDS) software.

For earlier versions of these release notes, refer to the *Intel SoC FPGA Embedded Development Suite Archives* section.

Related Information

Intel SoC FPGA Embedded Development Suite Archives on page 8
Provides a list of user guides for previous versions of the SoC FPGA EDS IP core.

Intel SoC FPGA Embedded Development Suite Intel Quartus® Prime version 19.1 Software Release

This section provides up-to-date information about the Intel SoC FPGA Embedded Development Suite software release for 19.1.

SoC EDS Professional Edition

The SoC EDS Professional Edition targets both the Intel Arria® 10 and Intel Stratix® 10 and must be used only with FPGA projects created in Intel Quartus® Prime Pro Edition.

What's New

- Linux* Host Support - Ubuntu 18.04
- Intel Stratix 10 SoC: U-Boot Expansion for Authentication support (>256 KB)
- Intel Stratix 10 Arm* Cortex*-A53 LLVM compiler is the non-GPL preloader compiler.
- For Microsoft* Windows* users, you need to manually install the Cygwin package for 64-bit Windows. For the link to the Cygwin download web page and the Intel-supported steps to install, go to Table 6 on page 5.

Tool Versions

Table 1. Pro Edition Tool Version Updates

Tools	Version
Arm Development Studio 5* (DS-5*) Intel SoC FPGA Edition	5.29.2
Linux Host Support - Ubuntu	18.04

Resolved Issues

Table 2. Resolved Issues

Area	Description
Golden Hardware Reference Designs for SoC FPGA Development Kits (GHRD)	• Fixed the hold violation in the Intel Arria 10 GHRD designs for both PR and non-PR. • Corrected the HPS Voltage (`MPU_CLK_VCCL`) `settings`

Enhancements

Table 3. Enhancements

Area	Description
Bootloader Generator and Bootloader	• Intel Stratix 10 SoC U-Boot: — Enabled authentication support for Intel Stratix 10 SoC U-Boot (FSBL and SSBL). — Added Partial Reconfiguration support from the Hard Processor System (HPS). — Ability to configure peripheral ECC security for Linux access. — Ability to handle SDRAM Double Bit Error (DBE) occurrence during Linux execution • Intel Stratix 10 SoC Arm Trusted Firmware (ATF) and UEFI: — Enabled ARMCLANG support for ATF. — Enabled kernel booting with PSCI call support.

Known Issues

Table 4. The generated Intel Stratix 10 HPS `handoff` file does not have the first four words of the `handoff` file header.

Description:	The generated Intel Stratix 10 HPS `handoff` file does not have the first four words of the `handoff` file header. This only occurs when the bootloader size is not 16 bytes aligned; and when using `quartus_cpf` in Intel Quartus Prime version 19.1.
Workaround:	Before injecting the bootloader to the SRAM Object File (`.sof`), ensure that the bootloader is 16 bytes aligned. You can use the `dd` command to copy several bytes to the bootloader binary before converting it to Intel Hex (IHEX), and ultimately using `quartus_cpf` to inject the particular bootloader to `.sof`.

Table 5. The Device Tree Generator that comes in Intel SoC FPGA EDS version 19.1 generates incorrect device tree data structure.

Description:	The Device Tree Generator (`sopc2dts`) in Intel SoC FPGA EDS version 19.1 generates incorrect device tree (DTS) for Intel Arria 10 Linux 4.14.73-ltis, specific to NAND boot.
Workaround:	Use the device tree that comes with Linux at `arm/boot/dts/socfpga_arria10_socdk_nand.dts`.

Table 6. Microsoft Windows users must follow the following steps to install the Cygwin package for 64-bit Windows.

Description:	Microsoft Windows users cannot follow the steps provided with the Cygwin install, you must follow the following steps in order to install the Cygwin package for 64-bit Windows, properly.
Workaround:	1. Download the latest 64-bit Cygwin installer from the Cygwin official website. *Note:* Be aware of the full path of the installer, you must use this path in the following step. 2. Open a windows terminal and copy the following command into the terminal, the colored portions need to be replaced: a. Under this folder <SoCEDS installation directory>\embedded \host_tools\, create a new folder named cygwin. *Note:* Replace this text with the SoC EDS installation directory. b. Run the following command from a Microsoft Windows command prompt: ***Attention:*** Copy the following command as a whole, ignore the fact that the long command is automatically separated into multiple lines. `<Path to Cygwin installer in Step 1>See Note. --quiet-mode --root \ <SoCEDS installation directory>\embedded\host_tools\cygwin --wait --site \ http://cygwin.mirrors.hoobly.com --packages make,gcc-core,gcc-g++,ncurses,\ inetutils,openssh,mosh,patch,flex,bison,tar,bzip2,zip,unzip,util-linux,git,\ subversion,vim,xxd,m4,wget,dos2unix,libintl-devel,diffutils,libncurses-devel,\ iperf,xorg-server,xinit,mingw64-x86_64-gcc-core,mingw64-x86_64-gcc-g++` *Note:* Replace <Path to Cygwin installer in Step 1> with the full path to the installer in step 1. 3. Wait until everything is automatically installed. For information about the command line and how each flag is used, refer to the Cygwin FAQ web page.

Intel SoC FPGA Embedded Development Suite Intel Quartus Prime version 18.1 Software Release

This section provides up-to-date information about the Intel SoC FPGA Embedded Development Suite software release for 18.1.

Related Information

Intel SoC FPGA Embedded Development Suite Archives on page 8
Provides a list of user guides for previous versions of the SoC FPGA EDS IP core.

SoC EDS Professional Edition

The SoC EDS Professional Edition targets both the Intel Arria 10 and Intel Stratix 10 and must be used only with FPGA projects created in Intel Quartus Prime Pro Edition.

Tool Versions

Table 7. Pro Edition Tool Version Updates

Tools	Version
Arm Compiler 5	5.06 update 6
Arm Compiler 6	6.10.1
Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition	5.29.1

continued...

Tools	Version
Linux Kernel	4.9.78-ltsi
Linux Compiler	4.8.3 (Linaro* GCC Snapshot 7.2-2017.11) 7.2.1 20171116
Mentor Graphics* Baremetal GCC Compiler	6.2.0 (Sourcery CodeBench Lite 2016.11-88)
Ångström	2018.06

Resolved Issues

Table 8. Resolved Issues

Area	Description
Bootloader Generator and Bootloader	• Intel Stratix 10 U-Boot: — U-Boot getting the SDRAM size using defines instead of calculations is fixed. — Driver disabling or enabling the QSPI controller too soon and inadvertently halting any ongoing flash read or write access is fixed. *Note:* This fix prevents the QSPI write intermittent issue from happening by ensuring the QSPI controller is always in idle mode after each read or write access. • Integer overflow flixed for Intel Arria 10. • Issue with ECC support not enabled causing UEFI to fail to boot is fixed. • U-Boot not booting when the Remote System Update (RSU) image is not found is fixed. *Note:* U-Boot does not update the Linux Device Tree Source (DTS) that is related to the RSU. So, Linux is aware there is no RSU support.

Enhancements

Table 9. Enhancements

Area	Description
Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition	Arm multi-core devices such as Cortex-A9 and Cortex-A53 part of our Intel FPGA SoC devices should flawlessly work with DS-5 Intel SoC FPGA Edition debugger when debugging on a multiprocessing environment for all supported SMP + AMP configurations.
Bootloader Generator and Bootloader	• Intel Stratix 10 U-Boot: — Enabled SDRAM ECC support if it's enabled in hardware design — Enabled SDRAM ECC error injection test code, for your validation purposes — Enabled Remote System Update support — Enabled Secure Monitor Call (SMC) support from all slave CPUs — Added Secure Monitor Call (SMC) support for EMAC setting, which allows the kernel to change the Ethernet controller properties — Added System MMU (SMMU) initialization which allows non-secure accesses with SMMU peripherals. The init code sets up stream ID for SMMU peripheral matching • Intel Stratix 10 Arm Trusted Firmware: — Enabled SDRAM ECC support if it is enabled in hardware design • Intel Stratix 10 UEFI: — Rebased UEFI code base to UDK2018 — Added GPIO driver support and control application — Updated Timer frequency so that the countdown seconds is accurate — Removed unused codes

Known Issues

Table 10. Why does the HPS lock up or EMIF calibration fails during cold reset if ECC is enabled on HPS-EMIF?

Description:	Either HPS locks up, EMIF calibration fails or both during cold-reset, if ECC is enabled on HPS-EMIF.
Workaround:	Disable **HPS_EMIF_ECC** in GHRD and SoCEDS. The problem is scheduled to be fixed in a future release of the Intel Quartus Prime Pro Edition software.

SoC EDS Standard Edition

The SoC EDS Standard Edition targets the Cyclone® V, Arria V and Intel Arria 10, and must to be used only with FPGA projects created in Intel Quartus Prime Standard Edition.

Tool Versions

Table 11. Standard Edition Tool Version Updates

Tools	Version
Arm Compiler 5	5.06 update 6
Arm Compiler 6	6.10.1
Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition	5.29.1
Linux Kernel	4.9.78-ltsi
Linux Compiler	4.8.3 (Linaro GCC Snapshot 7.2-2017.11) 7.2.1 20171116
Mentor Graphics Baremetal GCC Compiler	6.2.0 (Sourcery CodeBench Lite 2016.11-88)
Ångström	2018.06

Resolved Issues

Table 12. Resolved Issues

Area	Description
Bootloader Generator and Bootloader	Integer overflow flixed for Intel Arria 10.

Intel SoC FPGA Embedded Development Suite Archives

Intel Quartus Prime Version	Release Notes (PDF)
18.1	Intel SoC FPGA Embedded Development Suite Release Notes (18.1) These release notes cover Intel Quartus Prime versions 18.0 through 18.1.
18.0	Intel SoC FPGA Embedded Development Suite Release Notes (18.0) These release notes cover Intel Quartus Prime versions 17.0 through 18.0.

Document Revision History for Intel SoC FPGA Embedded Development Suite (SoC EDS) Release Notes

Table 13. Document Revision History for Intel SoC FPGA Embedded Development Suite (SoC EDS) Release Notes

Document Version	Changes
2019.04.10	• Added information about installing Cygwin for Microsoft Windows users. • Created the Intel SoC FPGA Embedded Development Suite Archives" section to contain all of the previous versions of these release notes. • Removed the Intel Quartus Prime 18.0 version from these release notes and added them to the "Intel SoC FPGA Embedded Development Suite Archives" section.
2018.09.24	• Updated the Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition version. • Added "Enhancements" and "Issues Resolved" for these areas in : — Golden Hardware Reference Designs for SoC FPGA Development Kits (GHRD) — Arm DS-5 Intel SoC FPGA Edition — Bootloader Generator and Bootloader

continued...

Document Version	Changes
2018.05.07	Added new features, bug fixes, enhancements, and known issues during the Intel Quartus Prime 18.0 release of the SoC FPGA EDS software - Standard and Pro editions.
2017.12.05	Added new features, bug fixes, enhancements, and known issues during the Intel Quartus Prime 17.1 release of the SoC FPGA EDS software - Standard and Pro editions.
2017.05.08	Release Notes divided into a Pro and Standard section.
2016.11.07	Added clarity to the early IO release feature.
2016.05.09	Added new features, bug fixes, enhancements, and known issues during the Intel Quartus Prime 16.0 release updates
2016.01.22	Added new features, bug fixes, enhancements, and known issues during the Intel Quartus Prime 15.1.1 release updates
2015.11.02	Added new features, bug fixes, enhancements, and known issues during the Intel Quartus Prime 15.1 release updates
2015.06.05	Added new features, bug fixes, enhancements, and known issues during the Intel Quartus Prime 15.0.1 release updates
2015.05.01	Added new features, bug fixes, enhancements, and known issues during the Intel Quartus Prime 15.0 release updates