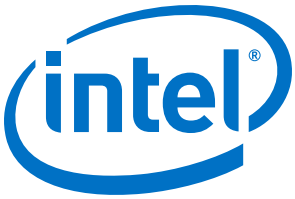

Intel® SoC FPGA Embedded Development Suite (SoC EDS) Release Notes

Updated for Intel® Quartus® Prime Design Suite: **18.1**

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Intel® SoC FPGA Embedded Development Suite (SoC EDS) 18.1 Release Notes

This document provides information about the SoC EDS Professional Edition and SoC EDS Standard Edition software release versions for the Intel® SoC FPGA Embedded Development Suite (SoC EDS).

This document consists of versions 18.0 through 18.1 of the Intel SoC FPGA Embedded Development Suite Release Notes.

For more information about versions 17.0 through 17.1, refer to *Intel SoC FPGA Embedded Development Suite Release Notes (2017)*.

Related Information

Intel SoC FPGA Embedded Development Suite Release Notes (2017)

18.1 Intel SoC FPGA Embedded Development Suite Software Release

This document provides up-to-date information about the Intel SoC FPGA Embedded Development Suite software release for 18.1.

SoC EDS Professional Edition

The SoC EDS Professional Edition targets both the Intel Arria® 10 SoC and Intel Stratix® 10 SoC and must be used only with FPGA projects created in Intel Quartus® Prime Pro Edition.

Tool Versions

Table 1. Pro Edition Tool Version Updates for 18.1 Release

Tools	Version
Arm* Compiler 5	5.06 update 6
Arm Compiler 6	6.10.1
Arm Development Studio 5* (DS-5*) Intel SoC FPGA Edition	5.29.1
Linux* Kernel	4.9.78-ltsi
Linux Compiler	4.8.3 (Linaro* GCC Snapshot 7.2-2017.11) 7.2.1 20171116
Mentor Graphics* Baremetal GCC Compiler	6.2.0 (Sourcery CodeBench Lite 2016.11-88)
Ångström	2018.06

Resolved Issues

Table 2. Resolved Issues in the 18.1 Release

Area	Description
Bootloader Generator and Bootloader	• Intel Stratix 10 SoC U-Boot: — U-Boot getting the SDRAM size using defines instead of calculations is fixed. — Driver disabling or enabling the QSPI controller too soon and inadvertently halting any ongoing flash read or write access is fixed. *Note:* This fix prevents the QSPI write intermittent issue from happening by ensuring the QSPI controller is always in idle mode after each read or write access. • Integer overflow fixed for Intel Arria 10 SoC. • Issue with ECC support not enabled causing UEFI to fail to boot is fixed. • U-Boot not booting when the Remote System Update (RSU) image is not found is fixed. *Note:* U-Boot will not update the Linux Device Tree Source (DTS) that is related to the RSU. So, Linux is aware there is no RSU support.

Enhancements

Table 3. Enhancements in the 18.1 Release

Area	Description
Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition	Arm multi-core devices such as Cortex*-A9 and Cortex-A53 part of our Intel FPGA SoC devices should flawlessly work with DS-5 Intel SoC FPGA Edition debugger when debugging on a multiprocessing environment for all supported SMP + AMP configurations..
Bootloader Generator and Bootloader	• Intel Stratix 10 SoC U-Boot: — Enabled SDRAM ECC support if it's enabled in hardware design — Enabled SDRAM ECC error injection test code, for your validation purposes — Enabled Remote System Update support — Enabled Secure Monitor Call (SMC) support from all slave CPUs — Added Secure Monitor Call (SMC) support for EMAC setting, which allows the kernel to change the Ethernet controller properties — Added System MMU (SMMU) initialization which allows non-secure accesses with SMMU peripherals. The init code sets up stream ID for SMMU peripheral matching • Intel Stratix 10 SoC Arm Trusted Firmware: — Enabled SDRAM ECC support if it is enabled in hardware design • Intel Stratix 10 SoC UEFI: — Rebased UEFI code base to UDK2018 — Added GPIO driver support and control application — Updated Timer frequency so that the countdown seconds is accurate — Removed unused codes

Known Issues

Table 4. Why does the HPS hang or EMIF calibration fails during cold reset if ECC is enabled on HPS-EMIF?

Description:	HPS hangs and/or EMIF calibration fails during cold-reset if ECC is enabled on HPS-EMIF.
Workaround:	Disable **HPS_EMIF_ECC** in GHRD and SoCEDS. The problem is scheduled to be fixed in a future release of the Intel Quartus Prime Pro Edition software.

SoC EDS Standard Edition

The SoC EDS Standard Edition targets the Cyclone® V SoC, Arria V SoC and Intel Arria 10 SoC, and must to be used only with FPGA projects created in Intel Quartus Prime Standard Edition.

Tool Versions

Table 5. Standard Edition Tool Version Updates for 18.1 Release

Tools	Version
Arm Compiler 5	5.06 update 6
Arm Compiler 6	6.10.1
Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition	5.29.1
Linux Kernel	4.9.78-ltsi
Linux Compiler	4.8.3 (Linaro GCC Snapshot 7.2-2017.11) 7.2.1 20171116
Mentor Graphics Baremetal GCC Compiler	6.2.0 (Sourcery CodeBench Lite 2016.11-88)
Ångström	2018.06

Resolved Issues

Table 6. Resolved Issues in the 18.1 Release

Area	Description
Bootloader Generator and Bootloader	Integer overflow fixed for Intel Arria 10 SoC.

18.0 Intel SoC FPGA Embedded Development Suite Software Release

SoC EDS Professional Edition

The SoC EDS Professional Edition targets both the Intel Arria 10 SoC and Intel Stratix 10 SoC and must be used only with FPGA projects created in Intel Quartus Prime Pro Edition.

Tool Versions

Table 7. Pro Edition Tool Version Updates

Tools	Version
Arm Development Studio 5 Intel SoC FPGA Edition	5.28.1
Linux Kernel	4.9.78-ltsi
Mentor Graphics Baremetal GCC Compiler	6.2
Ångström	2018.06

New Features

Table 8. New Features in the 18.0 Release

Area	Description
Arm Development Studio 5 Intel SoC FPGA Edition	Intel Arria 10 SoC SoC: The Bare-Metal Ethernet Example has been added
	Intel Stratix 10 SoC SoC: • Intel FPGA Download Cable II *Note:* For more information, refer to the KDB. • Linux boot path • Intel Stratix 10 SoC GHRD • HWLIBs Port in SoC EDS • Bare-Metal Ethernet and UART examples
Bootloader Generator and Bootloader	The following features were added: • Intel Stratix 10 SoC SoC Arm Trusted Firmware (ATF), an open source BSD-3 clause license secure monitor • Intel Stratix 10 SoC SoC U-Boot and UEFI

Resolved Issues

Table 9. Resolved Issues in the 18.0 Release

Area	Description
Bootloader Generator and Bootloader	Intel Stratix 10 SoC SoC: • There was an issue with the Intel Stratix 10 SoC SoC ATF Generic Interrupt Controller (GIC) setup. • The SPL times out waiting for the Mailbox ACK • Clock Manager driver to grab the clock source frequency from handoff binary blob instead of hard coding
	The Linux Symmetric Multi-Processing (SMP) feature is broken in U-Boot. **Fix:** Moved the secure code to the upper 128 K in OCRAM.
	Debugging timeout issue where watchdog is not paused when debugging with debugger. **Fix:** Updated to ensure that all watchdogs are paused when one of the CPU is in the debugging state.
Golden Hardware Reference Designs for SoC FPGA Development Kits (GHRD)	DDR calibration fails for Intel Stratix 10 SoC. **Fix:** Re-enabled DDR4 diagnostic options to work around Elpida-specific VREF Calibration issues.

continued...

Area	Description
	Incorrect Interrupt Latency Counter width caused the Linux driver to fail to load. **Fix:** Changed the Latency Counter width to 2.
	U-Boot does not launch after a reset is issued. **Fix:** Switching off FPGA Boot.
	Needed to update the Makefile for Intel Arria 10 SoC GHRD for simplified persona revision (PR).
	HPS wipe firmware needed to be updated to prevent the CIN address from rolling over beyond word 31.
	Intel Arria 10 SoC SoC • U-boot not launching after a reset is triggered • Incorrect DTB file name corrected
Golden System Reference Designs for SoC FPGA Development Kits (GSRD)	QSPI parameters, such as: `mtd0` missing from the Intel Arria 10 SoCDevelopement Kit XML file. **Fix:** Added `mtd0` to the xml file.
Hardware Libraries (HWLIBs)	Intel Arria 10 SoC SoC: Timer project does not resolve include paths
	The Intel Arria 10 SoC and Intel Stratix 10 SoC ethernet examples are missing launch files: `.cproject` and `.project`
	`alt_spi.c` is an unnecessary file in the ethernet example file causing an error. **Fix:** File removed.
	Recent change in the SPI API caused the SPI `lp-int-socfpga` test to fail.
	LUA example is not importing into Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition. **Fix:** Build from the commandline.
SoC EDS	Error message indicating that ARMClang cannot be found. **Fix:** Updated `.cproject` to include ARMClang as the default toolchain.
	Unfinished files included in the build causing errors.
	Error when using `alt_printf` with logging.
	Broken clean compile tests were causing errors.

Enhancements

Table 10. Enhancements in the 18.0 Release

Area	Description
Bootloader Generator and Bootloader	Intel Stratix 10 SoC SoC UEFI supports Intel Stratix 10 SoC SoC dev kit, enabled in SOCEDS 18.0.
	Intel Stratix 10 SoC SoC Arm Trusted Firmware (ATF) supports Cadence* QSPI controller and SDM mailbox.
	Intel Stratix 10 SoC SoC U-Boot supports:

continued...

Area	Description
	• FPGA configuration final solution, with better performance compared interim solution (For example, fine tuning in progress) • SDRAM ECC, including test code to inject ECC fault (For example, fine tuning in progress) • Watchdog, where cold reset is triggered if timeout occurred • Boot script, where customization can be done without modifying U-Boot source
	Intel Stratix 10 SoC SoC U-Boot, UEFI and ATF supports: • Cold reset, I^2C, SPI, and GPIO (work in progress for BSD bootloader) • Linux Symmetric Multi-Processing (SMP) through the Arm standard Power State Coordination Interface (PSCI)
	The first 16 MB of the SDRAM are reserved for the Intel Stratix 10 SoC FPGA configuration data block. The kernel image's load address is now started at 32 MB to ensure there is enough space between the 16 MB reserved block and the kernel image.
Golden Hardware Reference Designs for SoC FPGA Development Kits (GHRD)	HPS wipe firmware is now synched.

Known Issues

Table 11. Why do I see the license error (Error: C9555E: Failed to check out a license) for ARMCC or ARMCLANG when compiling from the command line?

Description:	SoC EDS Embedded Command Shell needs to know the license file location and tool variant.

Workaround:	To work around this problem set the following environment variables in the SoC EDS command shell before compiling or running make: (syntax shown is for BASH):
	`export ARM_TOOL_VARIANT=altera`
	`export ARMLMD_LICENSE_FILE='license-file-path'`
	More information regarding this environment variables and their values can be found on the Arm website.

Table 12. Intel FPGA Download Cable II support issue when using semihosting from command line

Description:	For the Intel FPGA Download Cable II support, there is an issue here with respect to the DS-5 Intel SoC FPGA Edition and Intel FPGA Download Cable II support. The issue is specific to the command line flow when using semihosting.
Workaround:	It is unlikely customers will be using Intel FPGA Download Cable II from the command line. Customers should contact us if they need a workaround.

Table 13. Minimal Bitstream Reconfiguration Failure

Description:	Using the serial flash loader without power cycling may cause configuration errors.
Workaround:	Power cycle before using the serial flash loader.

Table 14. Intel Stratix 10 SoC UEFI bootloader tarball in SoC EDS cannot be compiled nor used for booting Linux

Description:	Intel Stratix 10 SoC UEFI bootloader tarball in SoC EDS cannot be compiled nor used for booting Linux.
Workaround:	Grab Intel Stratix 10 SoC UEFI source from github: 1. `git clone https://github.com/altera-opensource/uefi-socfpga` 2. cd uefi-socfpga 3. git checkout socvp_socfpga_udk2015 4. Use the source to compile and boot as usual

Table 15. Ångström image inside SoC EDS SD image does not contain the patch for intermittent `ttyS0` boot issue

Description:	Ångström image inside SoC EDS SD image does not contain the patch for intermittent `ttyS0` boot issue.
Workaround:	Ensure you use the build and the Ångström image based on the GSRD build instead of from SoC EDS.

Related Information

Knowledge Base

For more information about known issues, enter keywords in the search bar to narrow your search.

SoC EDS Standard Edition

The SoC EDS Standard Edition targets the Cyclone V SoC, Arria V SoC and Intel Arria 10 SoC, and must to be used only with FPGA projects created in Intel Quartus Prime Standard Edition.

Tool Versions

Table 16. Standard Edition Tool Version Updates

Tools	Version
Arm Development Studio 5 Intel SoC FPGA Edition	5.28.1
Linux Kernel	4.9.78-ltsi
Mentor Graphics Baremetal GCC Compiler	6.2

Resolved Issues

Table 17. Resolved Issues in the 18.0 Release

Area	Description
Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition	As a result of updating Linux kernel 4.9LTSI, additional device tree parameters are needed in the bindings. **Fix:** The appropriate parameters have been added to the Cyclone V SoC, Arria V SoC, and Intel Arria 10 SoC GHRD board XML.
Hardware Libraries (HWLIBs)	FPGA example designs are not building for the Stardard edition.
	Recent change in the SPI API caused the SPI `lp-int-socfpga` test to fail.

continued...

Area	Description
Golden System Reference Designs for SoC FPGA Development Kits (GSRD)	QSPI parameters, such as: `mtd0` missing from the Intel Arria 10 SoCDevelopement Kit XML file. **Fix:** Added `mtd0` to the xml file.
SoC EDS	Git changes to HWLIBs need to be added to the Standard edition.
	The GHRD Intel Arria 10 SoC System Control Compatible Strings, LEDs, cnds, and read-delay need to be updated.

Enhancements

Table 18. Enhancements in the 18.0 Release

Area	Description
Intel SoC FPGA Embedded Development Suite	Updated the GHRD Arria 10 System Control Compatible Strings, LEDs, cnds, and read-delay
Hardware Libraries (HWLIBs)	• Git changes added • Failing example designs are now building • Add BOOT_FROM_FPGA to `config.mk` to indicate that MPL is running from the FPGA

Known Issues

Table 19. Why do I see the license error (Error: C9555E: Failed to check out a license) for ARMCC or ARMCLANG when compiling from the command line?

Description:	SoC EDS Embedded Command Shell needs to know the license file location and tool variant.

Workaround:	To work around this problem set the following environment variables in the SoC EDS command shell before compiling or running make: (syntax shown is for BASH):
	`export ARM_TOOL_VARIANT=altera`
	`export ARMLMD_LICENSE_FILE='license-file-path'`
	More information regarding this environment variables and their values can be found on the Arm website.

Table 20. The Hardware Libraries Minimal Preloader (MPL) design example is not present in the 18.0 Standard edition

Description:	The Hardware Libraries Minimal Preloader (MPL) design example is not present in the 18.0 Standard edition.
Workaround:	If you want to use MPL, you should use the version shipped with the 17.1 Standard edition.

Table 21. Ångström image inside SoC EDS SD image does not contain the patch for intermittent ttyS0 boot issue

Description:	Ångström image inside SoC EDS SD image does not contain the patch for intermittent **ttyS0** boot issue.
Workaround:	Do ensure you use build and use the Ångström image based on GSRD build instead from the SoC EDS.

Related Information

Knowledge Base
For more information about known issues, enter keywords in the search bar to narrow your search.

Document Revision History for Intel SoC FPGA Embedded Development Suite (SoC EDS) Release Notes

Table 22. Document Revision History for Intel SoC FPGA Embedded Development Suite (SoC EDS) Release Notes

Document Version	Changes
2018.09.24	• Updated the Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition version. • Added "Enhancements" and "Issues Resolved" for these areas in : — Golden Hardware Reference Designs for SoC FPGA Development Kits (GHRD) — Arm DS-5 Intel SoC FPGA Edition — Bootloader Generator and Bootloader
2018.05.07	Added new features, bug fixes, enhancements, and known issues during the 18.0 release of the SoC FPGA EDS software - Standard and Pro editions.
2017.12.05	Added new features, bug fixes, enhancements, and known issues during the 17.1 release of the SoC FPGA EDS software - Standard and Pro editions.
2017.05.08	Release Notes divided into a Pro and Standard section.
2016.11.07	Added clarity to the early IO release feature.
2016.05.09	16.0 release updates
2016.01.22	15.1.1 release updates
2015.11.02	15.1 release updates
2015.06.05	15.0.1 release updates
2015.05.01	15.0 release updates