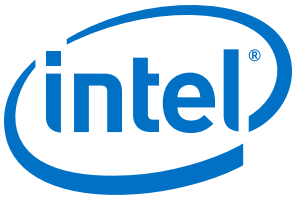

Intel® SoC FPGA Embedded Development Suite (SoC EDS) Release Notes

Updated for Intel® Quartus® Prime Design Suite: **18.0**

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Latest document on the web: **PDF** | **HTML**

Contents

1. Intel® SoC FPGA Embedded Development Suite (SoC EDS) Release Notes

These release notes cover versions 17.0 through 18.0 of the Intel® SoC FPGA Embedded Development Suite (SoC EDS) software releases.

Each section is divided into two sub-sections to cover the two editions offered in each release.

1.1. Intel SoC FPGA Embedded Development Suite Version 18.0 Release Notes

1. SoC EDS Professional Edition Version 18.0

Pro Edition Tool Version Updates

Tools	Version
Arm* Development Studio 5* Intel SoC FPGA Edition	5.28.1
Linux Kernel	4.9.78-ltsi
Mentor Graphics* Baremetal GCC Compiler	6.2
Ångström	2017.06

New Features

Table 1. New Features in the 18.0 Release

Area	Description
Arm Development Studio 5 Intel SoC FPGA Edition	Intel Arria® 10 SoC SoC: The Bare-Metal Ethernet Example has been added
	Intel Stratix® 10 SoC SoC: • Intel FPGA Download Cable II *Note:* For more information, refer to the KDB. • Linux boot path • Intel Stratix 10 SoC GHRD • HWLIBs Port in SoC EDS • Bare-Metal Ethernet and UART examples
Bootloader Generator and Bootloader	The following features were added: • Intel Stratix 10 SoC SoC Arm Trusted Firmware (ATF), an open source BSD-3 clause license secure monitor • Intel Stratix 10 SoC SoC U-Boot and UEFI

Issues Resolved

Table 2. Issues Resolved in the 18.0 Release

Area	Description
Bootloader Generator and Bootloader	Intel Stratix 10 SoC SoC: • There was an issue with the Intel Stratix 10 SoC SoC ATF Generic Interrupt Controller (GIC) setup. • The SPL times out waiting for the Mailbox ACK • Clock Manager driver to grab the clock source frequency from handoff binary blob instead of hard coding
	The Linux Symmetric Multi-Processing (SMP) feature is broken in U-Boot. **Fix:** Moved the secure code to the upper 128 K in OCRAM.
	Debugging timeout issue where watchdog is not paused when debugging with debugger. **Fix:** Updated to ensure that all watchdogs are paused when one of the CPU is in the debugging state.
Golden Hardware Reference Designs for SoC FPGA Development Kits (GHRD)	DDR calibration fails for Intel Stratix 10 SoC. **Fix:** Re-enabled DDR4 diagnostic options to work around Elpida-specific VREF Calibration issues.
	Incorrect Interrupt Latency Counter width caused the Linux driver to fail to load. **Fix:** Changed the Latency Counter width to 2.
	U-Boot does not launch after a reset is issued. **Fix:** Switching off FPGA Boot.
	Needed to update the Makefile for Intel Arria 10 SoC GHRD for simplified persona revision (PR).
	HPS wipe firmware needed to be updated to prevent the CIN address from rolling over beyond word 31.
	Intel Arria 10 SoC SoC • U-boot not launching after a reset is triggered • Incorrect DTB file name corrected
Golden System Reference Designs for SoC FPGA Development Kits (GSRD)	QSPI parameters, such as: `mtd0` missing from the Intel Arria 10 SoCDevelopement Kit XML file. **Fix:** Added `mtd0` to the xml file.
Hardware Libraries (HWLIBs)	Intel Arria 10 SoC SoC: Timer project does not resolve include paths
	The Intel Arria 10 SoC and Intel Stratix 10 SoC ethernet examples are missing launch files: `.cproject` and `.project`
	`alt_spi.c` is an unnecessary file in the ethernet example file causing an error. **Fix:** File removed.
	Recent change in the SPI API caused the SPI `lp-int-socfpga` test to fail.
	LUA example is not importing into Arm Development Studio 5 (DS-5*) Intel SoC FPGA Edition. **Fix:** Build from the commandline.
SoC EDS	Error message indicating that ARMClang cannot be found. **Fix:** Updated `.cproject` to include ARMClang as the default toolchain.

continued...

Area	Description
	Unfinished files included in the build causing errors.
	Error when using `alt_printf` with logging.
	Broken clean compile tests were causing errors.

Enhancements

Table 3. Enhancements in the 18.0 Release

Area	Description
Bootloader Generator and Bootloader	Intel Stratix 10 SoC SoC UEFI supports Intel Stratix 10 SoC SoC dev kit, enabled in SOCEDS 18.0.
	Intel Stratix 10 SoC SoC Arm Trusted Firmware (ATF) supports Cadence* QSPI controller and SDM mailbox.
	Intel Stratix 10 SoC SoC U-Boot supports: • FPGA configuration final solution, with better performance compared interim solution (For example, fine tuning in progress) • SDRAM ECC, including test code to inject ECC fault (For example, fine tuning in progress) • Watchdog, where cold reset is triggered if timeout occurred • Boot script, where customization can be done without modifying U-Boot source
	Intel Stratix 10 SoC SoC U-Boot, UEFI and ATF supports: • Cold reset, I^2C, SPI, and GPIO (work in progress for BSD bootloader) • Linux Symmetric Multi-Processing (SMP) through the Arm standard Power State Coordination Interface (PSCI)
	The first 16 MB of the SDRAM are reserved for the Intel Stratix 10 SoC FPGA configuration data block. The kernel image's load address is now started at 32 MB to ensure there is enough space between the 16 MB reserved block and the kernel image.
Golden Hardware Reference Designs for SoC FPGA Development Kits (GHRD)	HPS wipe firmware is now synched.

Known Issues

Table 4. Intel FPGA Download Cable II support issue when using semihosting from command line

Description:	For the Intel FPGA Download Cable II support, there is an issue here with respect to the DS-5 Intel SoC FPGA Edition and Intel FPGA Download Cable II support. The issue is specific to the command line flow when using semihosting.
Workaround:	It is unlikely customers will be using Intel FPGA Download Cable II from the command line. Customers should contact us if they need a workaround.

Table 5. Minimal Bitstream Reconfiguration Failure

Description:	Using the serial flash loader without power cycling may cause configuration errors.
Workaround:	Power cycle before using the serial flash loader.

Table 6. Intel Stratix 10 SoC UEFI bootloader tarball in SoC EDS cannot be compiled nor used for booting Linux*

Description:	Intel Stratix 10 SoC UEFI bootloader tarball in SoC EDS cannot be compiled nor used for booting Linux*.
Workaround:	Grab Intel Stratix 10 SoC UEFI source from github: 1. `git clone https://github.com/altera-opensource/uefi-socfpga` 2. cd uefi-socfpga 3. git checkout socvp_socfpga_udk2015 4. Use the source to compile and boot as usual

Table 7. Ångström image inside SoC EDS SD image does not contain the patch for intermittent `ttyS0` boot issue

Description:	Ångström image inside SoC EDS SD image does not contain the patch for intermittent `ttyS0` boot issue.
Workaround:	Ensure you use the build and the Ångström image based on the GSRD build instead of from SoC EDS.

Related Information

Knowledge Base

For more information about known issues, enter keywords in the search bar to narrow your search.

1.1.2. SoC EDS Standard Edition Version 18.0

Standard Edition Tool Version Updates

Tools	Version
Arm Development Studio 5 Intel SoC FPGA Edition	5.28.1
Linux Kernel	4.9.78-ltsi
Mentor Graphics Baremetal GCC Compiler	6.2

Issues Resolved

Table 8. Issues Resolved in the 18.0 Release

Area	Description
Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition	As a result of updating Linux kernel 4.9LTSI, additional device tree parameters are needed in the bindings. **Fix:** The appropriate parameters have been added to the Cyclone® V SoC, Arria V SoC, and Intel Arria 10 SoC GHRD board XML.
Hardware Libraries (HWLIBs)	FPGA example designs are not building for the Stardard edition.
	Recent change in the SPI API caused the SPI `lp-int-socfpga` test to fail.

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Area	Description
Golden System Reference Designs for SoC FPGA Development Kits (GSRD)	QSPI parameters, such as: `mtd0` missing from the Intel Arria 10 SoCDevelopement Kit XML file. **Fix:** Added `mtd0` to the xml file.
SoC EDS	Git changes to HWLIBs need to be added to the Standard edition.
	The GHRD Intel Arria 10 SoC System Control Compatible Strings, LEDs, cnds, and read-delay need to be updated.

Enhancements

Table 9. Enhancements in the 18.0 Release

Area	Description
Intel SoC FPGA Embedded Development Suite	Updated the GHRD Arria 10 System Control Compatible Strings, LEDs, cnds, and read-delay
Hardware Libraries (HWLIBs)	• Git changes added • Failing example designs are now building • Add BOOT_FROM_FPGA to `config.mk` to indicate that MPL is running from the FPGA

Known Issues

Table 10. The Hardware Libraries Minimal Preloader (MPL) design example is not present in the 18.0 Standard edition

Description:	The Hardware Libraries Minimal Preloader (MPL) design example is not present in the 18.0 Standard edition.
Workaround:	If you want to use MPL, you should use the version shipped with the 17.1 Standard edition.

Table 11. Ångström image inside SoC EDS SD image does not contain the patch for intermittent ttyS0 boot issue

Description:	Ångström image inside SoC EDS SD image does not contain the patch for intermittent **ttyS0** boot issue.
Workaround:	Do ensure you use build and use the Ångström image based on GSRD build instead from the SoC EDS.

1.2. Intel SoC FPGA Embedded Development Suite Version 17.1 Release Notes

1.2.1. SoC EDS Professional Edition Version 17.1

The SoC FPGA Pro Edition targets the Intel Arria 10 SoC SoC and must be used only with FPGA projects created in Intel Quartus® Prime Pro Edition.

Pro Edition Tool Version Updates

Tools	Version
Arm Development Studio 5 Intel SoC FPGA Edition	5.27.1
Arm Compiler 5	5.06 update 5
Arm Compiler 6	6.7.1
Linux Compiler	4.8.3 (Linaro GCC 4.8-2014.04)
Linux Kernel	4.1.33-ltsi
Mentor Graphics Bare-metal GCC Compiler	6.2.0

New Features

Table 12. New Features in the 17.1 Release

Area	Description
Golden Hardware Reference Design (GHRD)	Upgraded the `sysid` component so that it is Platform Designer compatible
	Added soft IP to support CMSIS
	For Cyclone V SoC SoC, SoC EDS 17.1 flash support was added
Bootloader Generator and Bootloader	For Intel Arria 10 SoC SoC U-Boot, semihosting support was added.

Issues Resolved

Table 13. Issues Resolved in the 17.1 Release

Area	Description
Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition	`Altera-SoCFPGA-HelloWorld-Bare-metal-ARMClang` software example importing incorrectly
Bootloader Generator and Bootloader	Receiving various Coverity critical security warnings including U-Boot common code.
	UEFI: • `git_clone.sh` script is failing • The UART output is distorted.
SoC EDS Toolchain	For Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition, the `Altera-SoCFPGA-Push-Button-Linux-GNU` project build is failing.
	SoC EDS Hello World Bare-metal project fails. **Fix:** Updated build configuration.

Enhancements

Table 14. Enhancements in the 17.1 Release

Area	Description
Bootloader Generator and Bootloader	Enhanced U-boot to support 2GB SDRAM

1.2.2. SoC EDS Standard Edition Version 17.1

The SoC EDS Standard Edition targets the Cyclone V SoC SoC, Arria V SoC SoC and Intel Arria 10 SoC SoC, and must to be used only with FPGA projects created in Intel Quartus Prime Standard Edition.

Standard Edition Tool Version Updates

Tools	Version
Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition	5.27.1
Arm Compiler 5	5.06 update 5
Arm Compiler 6	6.7.1
Linux Compiler	4.8.3 (Linaro GCC 4.8-2014.04)
Linux Kernel	4.1.33-ltsi
Mentor Graphics Bare-metal GCC Compiler	6.2.0

New Features:

Table 15. New Features in the 17.1 Release

Area	Description
Golden Hardware Reference Design (GHRD)	For Cyclone V SoC SoC, SoC EDS 17.1 flash support was added.

Issues Resolved

Table 16. Issues Resolved in the 17.1 Release

Area	Description
SoC EDS Toolchain	For Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition, the `Altera-SoCFPGA-Push-Button-Linux-GNU` project build is failing.
	Compile errors appeared after upgrading to GCC v6.2.0 U-Boot.
Nios2HAL EDS Toolchain	Intel Avalon® FIFO IP: • Incorrect back pressure behavior during reset state • Data loss when FIFO is almost full

Enhancements

Table 17. Enhancements in the 17.1 Release

Area	Description
Nios2EDS Toolchain	TSE/iniche driver to support `msgdma` updated to match the support provided in the Pro edition.
Hardware Libraries (HWLIBs)	Updated QSPI code

1.3. Intel SoC FPGA Embedded Development Suite 17.0 Release Notes

1.3.1. SoC EDS Professional Edition Version 17.0

Pro Edition Tool Version Updates

Tools	Version
Arm Development Studio 5 Intel SoC FPGA Edition	5.26.2
Linux Kernel	4.1.33-ltsi
Mentor Graphics Baremetal GCC Compiler	6.2.0

New Features

Table 18. New Features in the 17.0 Release

Area	Description
Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition	Bare-metal cheat sheets added
SoC FPGA Embedded Software	For the Linux Device Tree Generator (DTG), support was added for the TSE SGMII PCS.
	For the SOPC2DTS, Device Tree Compiler (DTC) no longer fails when the Display Port (DP) is initiated.
Bootloader Generator and Bootloader	Intel Arria 10 SoC U-Boot • I^2C driver is enabled • FPGA boot is enabled • Support for GCC6 is enabled • Multiport front end (MPFE) no longer hangs due to the transient clock • MAC address retrieved from EEPROM is enabled • SDRAM support up to 2 GB is enabled • SDRAM no longer fails initialization when ECC is enabled
	Intel Arria 10 SoC UEFI • Bad block marker implementation is no longer incorrect • MPFE no longer hangs due to the transient clock • NoC MPFE HPS lock issue fixed • Coverity static analysis security no longer generates a warning • Ability to setup the MAC address from an EEPROM value
Linux Device Tree Generator (DTG)	Triple Speed Ethernet (TSE) reference design hardware failure fixed
Golden Hardware Reference Design (GHRD)	Intel Arria 10 SoC GHRD: • Setup timing violation for PCIe Gen2x8, Gen3x4, and Gen3x8 fixed.
	For the DisplayPort GHRD, the resolution was updated from 640x480 to 1280x720.
	For GHRD Partial Reconfiguration (PR), the default value for the Display Port is no longer causing a generation/ compilation issue.
Golden System Reference Design (GSRD)	For Intel Arria 10 SoC DisplayPort GSRD hardware design, the display Port with terminal support was enabled.

continued...

Area	Description
	Resolution updated to 640x480 to fix the blanking issue observed by the DP Linux driver.
Toolchains	Includes Intel Stratix 10 SoC A53 Compiler (64-bit support) (1)
	Bare-metal GCC Compiler `newlib` error
Hardware Libraries (HWLIBs)	For Intel Arria 10 SoC, the SDRAM example was removed.
	For Arria V SoC MPL, the size needs to be reduced to allow compiling
	Compiling errors causing UEFI tests to fail
	There are MPL issues pertaining to the SD/MMC boot.

2. SoC EDS Standard Edition Version 17.0

New Features

Table 19. New Features in the 17.0 Release

Area	Description
Bootloader Generator and Bootloader	Intel Arria 10 SoC U-Boot • Enabled I^2C driver • Enabled support for GCC6 • Enabled FPGA boot

Issues Resolved

Table 20. Issues Resolved in the 17.0 Release

Area	Description
Bootloader Generator and Bootloader	For Intel Arria 10 SoC U-Boot, Network-on-chip (NoC) MPFE Hard Processor System (HPS) lock issue
	Intel Arria 10 SoC UEFI • NoC MPFE HPS lock issue fixed • MPFE hang issue due to transient clock fixed • Wrong bad block marker implementation fixed • Coverity static analysis security warning fixed
Golden Hardware Reference Design (GHRD)	For Intel Arria 10 SoC GHRD, the HPS SGMII design build fails `qsys-script` when receiving an invalid parameter from the transceiver PLL.
	Outdated information for the Arria V SoC and Cyclone V SoC SoC Development Kits. **Fix:** `soc_system_board_info.xml` file updated.
Hardware Libraries (HWLIBs)	For Arria V SoC MPL, the size needs to be reduced for armcc.
	`snprintf` needs to be defined.
	Design example in the GHRD does not blink the LED.

continued...

(1) Arm Bare-metal compiler included with DS-5 Intel SoC FPGA Edition.

Area	Description
	`mpl/boot-bare-metal-fpga` tests fail.
	Compiling errors are causing the UEFI tests to fail.
	HWLIB DMA test from OCRAM to SDRAM is failing.

Enhancements

Table 21. Enhancements in the 17.0 Release

Area	Description
Bootloader Generator and Bootloader	Intel Arria 10 SoC U-Boot: • Enabled MAC address retrieved from EEPROM • Enabled SDRAM support up to 2 GB
	For Intel Arria 10 SoC UEFI, the ability to setup the MAC address from an EEPROM value is now available.
Hardware Libraries (HWLIBs)	The MPL was updated.
	The SDRAM files were updated.

Known Issues

Table 22. SDRAM ECC not Supported in Early IO Boot

Description	The SDRAM ECC is not supported in Early IO release boot because DDR calibration failed after the peripheral RBF was programmed to the FPGA.
Workaround	No workaround. This does not impact the non Early IO release boot.

Table 23. Intel Bare-metal Folder Unavailable in SoCEDS-Arm DS-5 Intel SoC FPGA Edition CheatSheet

Description	The DS-5 Intel SoC FPGA Edition tool has been updated to have cheat sheets for Intel Bare-metal development. In some cases, the Linux version does not display these cheat sheets.
Workaround	Invoking Arm DS-5 Intel SoC FPGA Edition using `sudo` may allow the cheatsheets to appear.

Related Information

Knowledge Base

For more information about known issues, enter keywords in the search bar to narrow your search.

1.4. Document Revision History for Intel SoC FPGA Embedded Development Suite (SoC EDS) Release Notes

Table 24. Document Revision History for Intel SoC FPGA Embedded Development Suite (SoC EDS) Release Notes

Document Version	Changes
2018.05.07	Added new features, bug fixes, enhancements, and known issues during the 18.0 release of the SoC FPGA EDS software - Standard and Pro editions.
2017.12.05	Added new features, bug fixes, enhancements, and known issues during the 17.1 release of the SoC FPGA EDS software - Standard and Pro editions.

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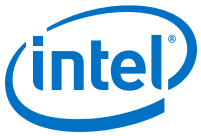

Document Version	Changes
2017.05.08	Release Notes divided into a Pro and Standard section.
2016.11.07	Added clarity to the early IO release feature.
2016.05.09	16.0 release updates
2016.01.22	15.1.1 release updates
2015.11.02	15.1 release updates
2015.06.05	15.0.1 release updates
2015.05.01	15.0 release updates