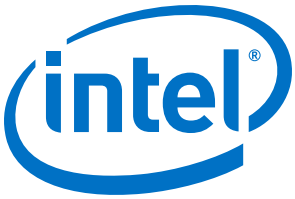

# Intel® Quartus® Prime Design Suite Version 18.1 Update Release Notes

Updated for Intel® Quartus® Prime Design Suite: **18.1.1**



RN-01080-18.1.1.0 | 2019.01.03
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Send Feedback

# 1. Intel® Quartus® Prime Design Suite Version 18.1 Update Release Notes

The *Intel® Quartus® Prime Design Suite Update Release Notes* describe the contents of Intel Quartus Prime Design Suite Version 18.1 software updates.

The Intel Quartus Prime Design Suite Version 18.1 updates apply only to Intel Quartus Prime Pro Edition.

### Related Information

- Intel Quartus Prime Pro Edition Software and Device Support Release Notes Version 18.1
- Intel Quartus Prime Standard Edition Software and Device Support Release Notes Version 18.1

# 2. Issues Addressed in Update 1

## 2.1. Intel Quartus Prime Pro Edition Software

### Intel Quartus Prime Software

- Starting in V18.1.1, you cannot set the following Advanced I/O Timing assignments as a global setting. You can still use these assignments as pin assignments.
  - OUTPUT_IO_TIMING_NEAR_END_VMEAS
  - OUTPUT_IO_TIMING_FAR_END_VMEAS
  - OUTPUT_IO_TIMING_ENDPOINT
  - BOARD_MODEL_NEAR_PULLUP_R
  - BOARD_MODEL_NEAR_PULLDOWN_R
  - BOARD_MODEL_NEAR_C
  - BOARD_MODEL_NEAR_SERIES_R
  - BOARD_MODEL_NEAR_TLINE_C_PER_LENGTH
  - BOARD_MODEL_NEAR_TLINE_L_PER_LENGTH
  - BOARD_MODEL_NEAR_TLINE_LENGTH
  - BOARD_MODEL_TLINE_C_PER_LENGTH
  - BOARD_MODEL_TLINE_L_PER_LENGTH
  - BOARD_MODEL_TLINE_LENGTH
  - BOARD_MODEL_FAR_SERIES_R
  - BOARD_MODEL_FAR_C
  - BOARD_MODEL_FAR_PULLUP_R
  - BOARD_MODEL_FAR_PULLDOWN_R
  - BOARD_MODEL_TERMINATION_V
  - BOARD_MODEL_NEAR_SERIES_C
  - BOARD_MODEL_NEAR_DIFFERENTIAL_R
  - BOARD_MODEL_FAR_DIFFERENTIAL_R

### Intel Quartus Prime Device Support

- Enabled advanced support for Intel Stratix® 10 1SG211H and 1SG166H device families.
- Enabled full support for Intel Stratix 10 1SM16BH, 1SM16CH, 1SM21BH, 1SM21CH, 1ST250E, and 1ST280E device families.
- Enabled SRAM object file (`.sof`) support for Intel Stratix 10 1ST280 and 1ST250 device families.
- The timing model status for Intel Stratix 10 1SG280H, 1SX280H, 1SG250H, 1SX250H, 1SG210H, 1SX210H, 1SG165H, 1SX165H, 1SG110H, 1SX110H, 1SG085H, and 1SX085H devices is now set to Final.
- The power model status for Intel Stratix 10 1SG280H, 1SX280H, 1SG250H, 1SX250H, 1SG210H, 1SX210H, 1SG165H, 1SX165H, 1SG110H, 1SX110H, 1SG085H, and 1SX085H devices is now set to Final.

### Intel Quartus Prime Compilation and Design Flows

- The Intel Quartus Prime Compiler uses a parallel IP generation scheme now by default. Previously, using parallel IP generation was optional.
- The Enable Early Place flow setting is not supported with "Compile Time" Optimization Mode. The Compilation Dashboard shows status failed for the Fitter (Early Place) module, because it has been skipped in the compilation flow.

### Fitter

- Fixed bug with overly restrictive placement check for preserved logic in an incremental compile.
- Improved estimation of Hyper-Registers for device limit resource checking.
- Improved compile time in Quartus placement for Windows.
- Removed “Optimize for High Utilization” option from the “Physical Placement Effort” setting. Changes to improve placement for high utilization designs were incorporated into the default compilation flow.
- Improved compiler to use more accurate estimation for clock resources at the row level thus helping to avoid errors in routing.
- Fixed an issue that could cause the following fitter error to be incorrectly printed in incremental compilations when global signals are driven to partitions and left unused.

```
Error (18974): Signal is constrained to be routed locally to
destination(s), but signal must be routed globally
```

- The Enable Early Place flow setting is not supported with "Compile Time" Optimization Mode. The Compilation Dashboard shows status failed for the Fitter (Early Place) module, because it has been skipped in the compilation flow.
- Fixed incorrect bit settings for 8LUT LUTMASKs in cases where the fitter performs optimizations on them.

### Partial Reconfiguration

- Compilation support added to support a hardware issue affecting Intel Arria® 10 10AX16-10AX32 and 10AS16-10AS32 device families and Intel Cyclone® 10 devices that use Partial Reconfiguration or EDCRC. The changes ensure that resources that might be susceptible to glitches are not used during these compilations.
- For Intel Stratix 10 devices, a POF ID feature is added to help you with PR bitstream incompatibility checks. This feature is turned on by default. To enable this feature for an existing design, you must recompile the design and regenerate your bitstream using Version 18.1.1. PR POF ID must be enabled if you want to enable PR authentication. The maximum number of PR regions is 32 with PR POF ID enabled.

### Platform Designer

- Fixed the Parameters tool, which would continuously flicker after changing a parameter, for some video IPs, such as the Color Plane Sequencer II, and Color Space Converter II.
- Platform Designer uses a parallel IP generation scheme now by default. Previously, using parallel IP generation was optional.

### Power Analyzer

- For Intel Stratix 10 L-tile devices, the power model is updated for VCCIO3V rail. For details, see the Intel FPGAs and Programmable Devices Knowledge Base.
- The power model status for Intel Stratix 10 1SG280H, 1SX280H, 1SG250H, 1SX250H, 1SG210H, 1SX210H, 1SG165H, 1SX165H, 1SG110H, 1SX110H, 1SG085H, and 1SX085H devices is now set to Final.

### Programmer

- For Intel Stratix 10 devices, fixed the JAM/JBC syntax error for 2 Gb QSPI flash.
- Fixed an internal error that occurred in the Programmer GUI when autodetecting the EPCQA and S25FL flash.
- Fixed an issue where flash smaller than 128 Mb was not detected automatically.
- The complete Design Hash value in `.sof` file can now be found in the Compilation report, under Assembler -> Device Option -> Design hash.
- Fixed an error in the Intel Stratix 10 signing tool, which might cause unexpected behavior when the signing tool hashes the data.
- Fixed an unexpected closing of the Programmer GUI when an error occurred in the signing tool.
- For Intel Stratix 10 devices, added support for RSU upgrade and PR compatibility check.
- For Intel Stratix 10 devices, added support for signing certificates and allowing key cancel ID of 32-63.

### Timing Models

- For Intel Stratix 10 devices, the timing model is updated. For details, see the Intel FPGAs and Programmable Devices Knowledge Base.
- The timing model status for Intel Stratix 10 1SG280H, 1SX280H, 1SG250H, 1SX250H, 1SG210H, 1SX210H, 1SG165H, 1SX165H, 1SG110H, 1SX110H, 1SG085H, and 1SX085H devices is now set to Final.

## 2.2. IP and IP Cores

### 40G Ethernet IP Core

- Fixed an error with the reconfiguration arbitration logic in the hardware example top-level file.

### DisplayPort IP Core

- For Intel Stratix 10 devices, enabled Pixel Clock Recovery function.
- Changed Synopsys Design Constraints to entity-based Synopsys Design Constraints.
- Cleaned up compilation warnings found in Intel Stratix 10 design example with pixel clock recovery.
- Enabled Intel Stratix 10 design example with Pixel Clock Recovery variant.
- Enabled initiation of Tx in software regardless of the setting of DP_SUPPORT_EDID_PASSTHRU.
- Fixed an Intel Arria 10 design example when no display output occurred in non GPU mode.
- Enabled extended receiver capabilities when the maximum link rate is HBR3.
- For Intel Stratix 10 H-Tile devices, added VID_OPERATION_MODE "PMBUS MASTER" and PWRMGMT settings to the video connectivity design example IP `.qsf` file to enable Intel Stratix 10 SmartVID and power management capabilities.

### External Memory Interface IP Cores

- For Intel Cyclone 10 devices, enabled DDR3x72 support for 10CX085 FBGA672 devices.
- For Intel Stratix 10 devices, added support for DDR4 clamshell layout.

### Fixed Point Functions Intel FPGA IP Core

- The Fixed Point Functions Intel FPGA IP depends on the `dspip_recipes` library, which was unintentionally removed in Intel Quartus Prime Pro Edition Version 18.1. The `dspip_recipes` library has been restored in Version 18.1.1.

### HDMI IP Core

- For Intel Stratix 10 H-Tile devices, added VID_OPERATION_MODE "PMBUS MASTER" and PWRMGMT settings to the video connectivity design example IP `.qsf` file to enable Intel Stratix 10 SmartVID and power management capabilities.

### High Bandwidth Memory Interface IP Core

- Enabled Intel Stratix 10 MX production devices.

### High Speed Serial Interface (HSSI) IP Core

- Some configurations of the Intel Stratix 10 Transceiver IP with multiple reconfiguration profiles enabled might have more pessimistic timing analysis on data transfers between the transceivers and main fabric. Run the Version 18.1.1 Timing Analyzer on such designs to ensure timing closure.
- Improved timing driven placement and routing support for reconfigurable HSSI designs.
- Disabled the use of hyper-pipeline registers in the GUI.

### Intel Stratix 10 E-Tile Transceiver Native PHY IP Core

- Fixed signal connections for manual reset mode.
- Fixed the reset IP option to enable individual channels when individual Tx/Rx is enabled.
- Disabled the following GUI options:
  - **Enable TX fast pipeline registers**
  - **Enable RX fast pipeline registers**
- Updated the ical and pcal tuning parameters.
- Improved PHY performance in 3m DAC cables.
- Enabled BTI protection on the unused slave channels for dual-channel PAM4 Native PHY instances.

### Intel Stratix 10 L-Tile/H-Tile Transceiver Native PHY IP Core

- Removed a redundant character that caused warning message.
- Fixed an issue where an incorrect clock might be used when AN mode switches to data mode.

### Interlaken (2nd Generation) Intel Stratix 10 FPGA IP Core

- Added multi-segment mode support.
- Added **Number of Segments** parameter.
- Added support for lane and data rate combinations as follows:
  - For Intel Stratix 10 L-tile devices:
    - 4 lanes with 12.5/25.3/25.8 Gbps lane rates
    - 8 lanes with 12.5 Gbps lane rates
  - For Intel Stratix 10 H-tile devices:
    - 4 lanes with 12.5/25.3/25.8 Gbps lane rates
    - 8 lanes with 12.5/25.3/25.8 Gbps lane rates
    - 10 lanes with 25.3/25.8 Gbps lane rates
  - For Intel Stratix 10 E-tile (NRZ) devices:
    - 4 lanes with 6.25/12.5/25.3/25.8 Gbps lane rates
    - 8 lanes with 12.5/25.3/25.8 Gbps lane rates
    - 10 lanes with 25.3/25.8 Gbps lane rates
    - 12 lanes with 10.3125 Gbps lane rate
- Added the following new transmit user interface signals:
  - itx_eob1
  - itx_eopbits1
  - itx_chan1
- Added the following new receiver user interface signals:
  - irx_eob1
  - irx_eopbits1
  - irx_chan1
  - irx_err1
  - irx_err

### SDI II Intel FPGA IP Core

- For Intel Stratix 10 H-Tile devices, added VID_OPERATION_MODE "PMBUS MASTER" and PWRMGMT settings to the video connectivity design example IP `.qsf` file to enable Intel Stratix 10 SmartVID and power management capabilities.

## 2.3. DSP Builder for Intel FPGAs

- Single-precision floating-point adders in a DSP Builder design can now use a mixture of hard and soft implementations.
- VFFT_btb and VFFT_Light_btb blocks have been added. These support back-to-back operation of the variable-size FFT, so there is no need to flush the FFT pipeline between different-size FFT iterations.
- A defect in the VFFT_cp_btb and VFFT_Light_cp_btb blocks has been corrected. When the 18.1 versions of these blocks were used with multiple subchannels, the output start-of-packet, size and (for VFFT_cp_btb) end-of-packet signals were not correctly synchronized with the output valid signal.
- The optimization of floating-point scalar products is now slightly less aggressive. With default settings, DSP Builder no longer attempts to infer a chain-in input for scalar products. As a result of this change, complex scalar products now consume slightly more DSP blocks but require fewer logic resources for latency-balancing.
- Fixed initialization of SharedMems of type single precision float.
- Added support for loop blocks to the Advanced C-model feature.

## 2.4. Intel High Level Synthesis Compiler

- The Intel HLS Compiler now merges identical read access to an array. Previously, you had to explicitly merge identical array accesses.
- Added the HLS_SYNTHESIS macro. Statements in your component guarded by this macro work in x86 emulations but are disabled when compiling your component to an FPGA architecture.
- The `HLS/iostream.h` header file is deprecated. To use C++ standard output streams in your component, use the standard <iostream> header file and guard the output statements with the new HLS_SYNTHESIS macro.
- Fixed simulation failures that occurred when components or component parameters have names that are not unique or that conflict with reserved RTL keywords.
- Removed the misleading warning `Warning:-march has no effect. Using setting from -c compile` when using i++ to link object files.
- Fixed issues with `#pragma ivdep` which might cause a segmentation fault when the pragma is used with array clauses.
- Updated the `ac_int_basic_ops` tutorial to use `-std=c++14`.
- Fixed bugs in the ac data types provide with the Intel HLS Compiler.
- Replaced deprecated system call (fopen) on Windows for YUV2RGB example design.

## 2.5. Intel FPGA SDK for OpenCL*

- Fixed an error that occurred when reading data from a channel directly into the `__local` address space.
- Fixed an issue preventing some diagnostic messages from printing when you compiled kernel code for the fast emulator platform. In some rare cases, kernel compilations for the fast emulator failed without printing any useful error messages.
- Fixed an issue where all pointer parameters in OpenCL* kernels were incorrectly marked as `__restrict`.
- Fixed an issue where, in complex scenarios, a channel read in an `autorun` kernel might have forwarded data too soon.
- Removed `cl_khr_3d_image_writes` from the list of extensions advertised by the Intel FPGA SDK for OpenCL Runtime. This extension was advertised by mistake in previous releases.
- Fixed a bug that cause a crash when using multiple channels.
- Increased the maximum number of allowable identical abbreviated file names in OpenCL kernels from 1000 to 1000000.
- Set the INTELFPGA_CL macro to the version number of the compiler to enable users to version their code based on compiler version.
- Fixed issues with `#pragma ivdep` which might cause a segmentation fault when the pragma is used with array clauses.
- For Intel Stratix 10 devices, improved the stability of the OpenCL incremental compilation.
- Fixed an incremental compilation bug caused by an internal naming issue.
- Fixed an issue in the RTE where the `aocl version` command returned the following error:

```
aocl: Detailed error: Could not determine the path to SDK internal
libraries
```

*OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission of the Khronos Group™.

# 3. Software Issues Resolved

**Table 1. Customer Service Requests Resolved in Intel Quartus Prime Design Suite Version 18.1 Update 1**

| Customer Service Request Numbers Resolved | | | | | |
|---|---|---|---|---|---|
| 258070 | 279317 | 284801 | 285483 | 288834 | 288935 |
| 289150 | 289156 | 289247 | 289828 | 290489 | 290795 |
| 290795 | 299523 | 325248 | 325364 | 325577 | 325596 |
| 342569 | 342920 | 351062 | 351151 | 351169 | 351423 |
| 368992 | 379741 | 385968 | 386469 | 386832 | 387070 |
| 387390 | 387692 | 387924 | 388249 | 388711 | 388877 |
| 388932 | 388953 | 389869 | 391472 | 391472 | 391946 |
| 392019 | 392572 | 392897 | 393535 | 393543 | 393997 |
| 394967 | 395263 | 395631 | 395885 | 396112 | 11284795 |
| 11387341 | 11409998 | 11412747 | 11413470 | 11413677 | 11415210 |
| 11417550 | | | | | |

# 4. Software Patches Included in Update Releases

**Table 2. Intel Quartus Prime Pro Edition Software Patches included in Intel Quartus Prime Design Suite Version 18.0 Update 1**

| Software Version | Patch | Customer Service Request Number |
|---|---|---|
| Intel Quartus Prime V18.1 | 0.23 | 392897 |
| Intel Quartus Prime V18.1 | 0.17 | 290795 |
| Intel Quartus Prime V18.1 | 0.14 | 388249 |
| Intel Quartus Prime V18.1 | 0.13 | 325364 |
| Intel Quartus Prime V18.1 | 0.11 | - |
| Intel Quartus Prime V18.1 | 0.08 | - |
| Intel Quartus Prime V18.1 | 0.07 | - |
| Intel Quartus Prime V18.1 | 0.05 | - |
| Intel Quartus Prime V18.1 | 0.02 | - |
| Intel Quartus Prime V18.1 | 0.01p | - |
| Intel Quartus Prime V18.1 | 0.01dp3 | - |
| Intel Quartus Prime V18.0.1 | 1.41 | 388249 |
| Intel Quartus Prime V18.0.1 | 1.40 | 11412747 |
| Intel Quartus Prime V18.0.1 | 1.39 | - |
| Intel Quartus Prime V18.0.1 | 1.38 | - |
| Intel Quartus Prime V18.0.1 | 1.27 | |
| Intel Quartus Prime V18.0.1 | 1.14 | 288834 |
| Intel FPGA SDK for OpenCL V18.1 | 0.16cl | - |

# 5. Known Issues and Workarounds

### Known Issues and Workarounds for Intel Quartus Prime Pro Edition Version 18.1 Update 1

**Table 3.**

| Description | Workaround |
|---|---|
| For the Intel Stratix 10 1ST210 E-tile device family, you cannot configure the device from AVST x16 or AVST x32. | Configure the device using AVST x8. |

For information about other known software issues, visit the Intel FPGA Knowledge Base.

### Related Information

- Intel FPGA Knowledge Database
- Intel FPGA Documentation: Release Notes
- Intel FPGA Support Resources

# A. Document Revision History for Intel Quartus Prime Design Suite Update Release Notes

| Document Version | Intel Quartus Prime Version | Changes |
|---|---|---|
| 2019.01.03 | 18.1.1 | In IP and IP Cores on page 7, corrected the name of the *SDI II Intel FPGA IP Core*.<br>Previously, this IP core was listed as *Serial Data Interface (SDI) IP Core* |
| x2018.12.24 | 18.1.1 | Initial release with Intel Quartus Prime Design Suite version 18.1 Update 1 information. |