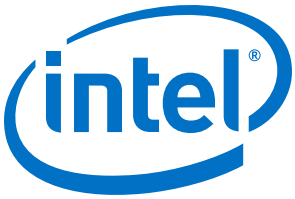

Intel® Quartus® Prime Design Suite Update Release Notes

Updated for Intel® Quartus® Prime Design Suite: **17.1.1**


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Contents

1 Intel® Quartus® Prime Design Suite Version 17.1 Update Release Notes

The *Intel® Quartus® Prime Design Suite Update Release Notes* describe the contents of Intel Quartus Prime Design Suite Version 17.1 software update 1.

Intel Quartus Prime Design Suite software updates require Version 17.1 of one of the following software packages:

- Intel Quartus Prime Pro Edition
- Intel Quartus Prime Standard Edition
- Intel Quartus Prime Lite Edition

You must have one of these editions of Intel Quartus Prime software installed before you can install the software updates.

If you use Intel Quartus Prime Lite Edition software, apply the Intel Quartus Prime Standard Edition software update. The Intel Quartus Prime Standard Edition software issues addressed in this update also apply to the device families that are supported by Intel Quartus Prime Lite Edition software.

Related Links

- Intel Quartus Prime Standard Edition Software and Device Support Release Notes Version 17.1
- Intel Quartus Prime Pro Edition Software and Device Support Release Notes Version 17.1

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2 Issues Addressed in Update 1

2.1 Intel Quartus Prime Pro Edition Software

Intel Quartus Prime Software

- Intel Quartus Prime software now assigns an installed device family as the default family when you create a new Quartus project.
- During compilation retiming, relaxed the legality check of SCL usage, Clock Enable Hyper-Register usage, or both for ROM designs that utilizes MLAB blocks.

Intel Quartus Prime Software GUI

- Added **Allow SEU fault injection** option to device settings for Intel Stratix® 10 devices.
- For Intel Stratix 10 devices, fixed Resource Property Viewer to show correct I/O usage.
- In Pin Planner GUI, corrected the display of rising edge and failing edge symbol for positive and negative clock of both UIB_PLL_REF_CLK and ESRAM clock respectively.
- Fixed an issee where Interface Planner does not work when launched from the GUI.

Intel Quartus Prime Device Support

- Enabled programmer object file (`.pof`) support for Intel Stratix 10 GX 2500 and GX2800 device families.
- Updated transceiver calibration firmware for Intel Stratix 10 devices.
- Updated configuration firmware for Intel Stratix 10 devices.
- Added support for the following Intel Arria® 10 GT devices:
  - 10AT090S2F45E2SG
  - 10AT115S2F45E2SG
- For Intel Stratix 10 devices, updated GXB_GND* description in the header of pin file and change unused rx/refclk pin from GND to GXB_GND* for Nadder family.
- Fixed an issue that prevented you from using 3 V I/O banks without instantiating transceivers on the tiles that support 3 V I/O.

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Intel Quartus Prime Compilation and Design Flows

- Changed hierarchical partial reconfiguration (HPR) flow scripts and non-HPR flow scripts for Intel Arria 10 and Intel Stratix 10 devices.
- Enabled partial reconfiguration bitstream generation for Intel Stratix 10 devices.
- Corrected the list of project-level SDC files not included in a Partition Database File (`.qdb`), during QDB export:

  ```
  Warning(19459)... The following SDC files will not be included:
  ```

- Added critical warning message for Intel Arria 10 and Intel Cyclone® 10 GX partial reconfiguration if a root partition is exported without excluding the reconfigurable partition.
- Made an update to avoid an internal error that might occur on any design using LABs.
- For Intel Stratix 10 devices, enabled back-annotation of timing information for detailed power analysis.
- For Intel Stratix 10 devices, fixed an issue where Intel Arria 10 was displayed in messages for the Intel Stratix 10 partial reconfiguration flow.
- Fixed CDR behavioral simulation model for stable recovered clock.
- Fixed an Abnormal Exit (Segment Violation) that can occur while trying to add post-fit Signal Tap on a node at a partition boundary for a design with PR partitions.
- Added a fix for partial reconfiguration on Intel Stratix 10 devices.
- For Intel Stratix 10 devices, added a post-placement check to issue a critical warning if PCIe, and OTN/SDI are placed within the same transceiver tile for H-Tiles.

Fitter

- For PCIe x1 designs, removed an invalid critical warning (19254).
- Reduced current and power consumption of some unused transceiver clock resources.
- Added Quartus Settings File (QSF) support for Intel Cyclone 10 GX devices.
- Disabled `gt_channel_rule` to support GT channels in RX simplex mode.
- Fixed a fitter issue with core clocks in incremental compilations that could result in an error similar to the following example error:

  ```
  Internal Error: Sub-system: PTI, File:
  /quartus/tsm/pti/pti_advanced_spice_rc_body.cpp, Line: 5376
  ```

- Fixed a fitter issue related to clocks locked to non-dedicated pins driving some types of periphery nodes, resulting in the following error:

  ```
  Internal Error: Sub-system: PCC, File:
  /quartus/periph/pcc/pcc_env.cpp, Line: 1394
  ```

- Fixed an issue where the fitter would generate an internal error for a specific configuration of ALMs that use dedicated feedback paths.
- Fixed an internal error in the fitter resynthesis algorithm caused by combinational loops through carry chains.

- Fixed an internal error that can occur when all integer DSPs are locked but there are unconstrained floating point DSPs in the design.
- For Intel Stratix 10 devices, fixed an internal error for designs with HBM or HSSI IP with complex settings when using preservation flows.
- Enable the Quartus Fitter retiming stage to retime register across RAM and ROM blocks to improve timing closure.
- Run time improvements to the Quartus Fitter retime stage.
- Reduce the Quartus fit run time on large designs that have many clock transfers, SDC exceptions, or both.
- For Intel Stratix 10 devices, fixed an internal error in the CDB_ATOM subsystem that can occur in designs with multiple core driven clocks in the same clock sector.
- Fixed bug related to clocks locked to non-dedicated pins driving some types of periphery nodes.
- Increased the number of clocks that the fitter automatically promotes from 128 to 1024.
- Fixed a fitter error where a small number of dual-purpose programming pins can be incorrectly classified as requiring GPIO pins, causing the following error message to get printed when it should not be:

```
Error(179000): Design requires 1160 user-specified I/O pins --
too many to fit in the 1152 user I/O pin locations available in the
selected device
```

- Improved the Fitter QoR.
- Enabled autoplacement of GT channels.
- For Intel Stratix 10 devices, fixed an error caused by register unpacking from DSP that has `accumulate` or `loadconst` inputs.
- Added a critical warning to avoid Intel Arria 10 PCS channel bonding hold violation.
- For Intel Stratix 10 devices, fixed a problem with a long runtime during timing analysis.
- Fixed the following error:

```
Internal Error: Sub-system: VPR20KMAIN, File:
/quartus/fitter/vpr20k/nf_arch/nf_net_rr_terminals.c, Line: 507
```

Platform Designer (formerly QSys)

- Fixed an issue where subsystems lost their exported interfaces on save when the system running Platform Designer is under load.
- Fixed an issue where running the `qsys-generate` command with both the `--simulation` and `--testbench` options together would cause the testbench to be created for the default device family instead of the target device family.
- Resolved an issue where the `qsys-script` command created a new Quartus project with a default device instead of the specified device in the `qsys-script .tcl` file.

Power Analyzer

- Change the leakage power for the following Intel Arria 10 parts: 10AS022xxxxxxxVx, 10AS016xxxxxxxVx, 10AX022xxxxxxxVx, 10AX016xxxxxxxVx, 10AS032xxxxxxxVx, 10AS027xxxxxxxVx, 10AX032xxxxxxxVx, 10AX027xxxxxxxVx, 10AS048xxxxxxxVx, 10AS048xxxxxxxVx
- Updated power models for Intel Stratix 10 devices.

Programmer

- For Intel Stratix 10 devices, enabled the generation of Advanced SEU Detection `.smh` files.
- For Intel Cyclone 10 GX devices, fixed an issue causing the configuration of the serial flash loader (SFL) to fail.
- For Intel Stratix 10 SoC devices, fixed an issue where a byte of data is missing from the device bootloader hexadecimal reading.

Synthesis

- Fixed an internal error in the router.
- Fixed an issue where in some cases, when assigning a `noprune` attribute to a wire connected the output of an instance, the `noprune` attribute would incorrectly apply to all nodes in that instance.
- For Intel Arria 10 devices, fixed clock and reset port name mapping errors when Avalon interfaces are enabled.
- Prevented an internal error when handling potentially corrupted databases:

```
Internal Error: Sub-system: QDB, File:
/quartus/db/qdb/qdb_service.cpp
```

- Fixed an internal error in place and route caused by a redundant LUT.
- For Intel Arria 10 devices, fixed an issue where some source-level assignments were ignored on nodes declared inside unnamed VHDL generate block.
- Added a signal to be used in the generate block for memory inference in SC FIFO module. This signal allows logic optimization and memory inference when the same signal is used across two generate statements.

Timing Closure

- Fixed Stratix 10 LUTRAM ES timing model
- Improved hold timing closure.

Timing Models

- Updated timing models for Intel Stratix 10 devices, including the Intel Stratix 10 GX2500, GX2800, SX2500, and SX2800 device families.
- For Intel Stratix 10 devices, reduced Quartus memory requirements and run time for designs that containing DSP blocks.
- Added initial Intel Stratix 10 production model timing support.
- Improved hold timing closure for Intel Stratix 10 devices.
- Fixed the following Internal Error:

```
Internal Error: Sub-system: TDC, File:
/quartus/tsm/tdc/tdc_accessories_delay_budget.cpp, Line: 1372
```

- Fixed the following Internal Error:

```
Internal Error: Sub-system: RTM, File:
/quartus/tsm/rtm/rtm_flow.cpp, Line: 3173
```

Timing Analyzer (formerly TimeQuest Timing Analyzer)

- Fixed issues with entity-bound SDC files. The first issue affected use of read_sdc -instance. The second issue affected cases where library was not specified for the entity.
- Fixed an issue with use of the TIMEQUEST_REPORT_SCRIPT assignment that might have caused an internal error.
- For Intel Stratix 10 devices, fixed a problem with a long runtime hang during placement.

Transceiver Toolkit

- Updated GUI adaption parameter naming to match Native PHY.
- Updated RX adaptation bit settings to match Native PHY.
- Improved speed and interpolation for HeatMap view.
- Added C2P RevB support.
- Corrected an issue with manually creating links.

Advanced Link Analyzer (formerly JNEye)

- Made the following updates:
  - Updated COM template for CEI-56G-LR/MR-PAM4
  - Fixed Pattern Designer simulation crash bug
  - Fixed IBIS-AMI statistical mode impulse response bug
  - Fixed TX SNDR calculation bug

2.2 Intel Quartus Prime Standard Edition Software

Intel Quartus Prime Software GUI

- Fixed an issue where Voltage and Temperature pages of Setting dialog crashed if you modified the option values after switching devices in Device Setting Dialog.
- Fixed an issue where the State Machine Viewer did not show the correct state diagram for designs that involved the LessThan operator.
- Fixed an issue where the location assignment labels were not displayed although **Show Location Assignments** was selected. Assignment labels are now shown correctly when you select **Show Location Assignments**.

Intel Quartus Prime Device Support

- Introduced support for Intel MAX® 10 U324 (10M02, 10M04, 10M08, and 10M16) package single power supply devices.

Fitter

- Resolved Fitter error caused by design hierarchy issue.

Programmer

- Fixed an issue that generated the following error message when programming the volatile key using a cable that does not support TCK clock configuration:

```
Unexpected error in JTAG server --error code 126
```

Power Analyzer

- Change the leakage power for the following Intel Arria 10 parts: 10AS022xxxxxxxVx, 10AS016xxxxxxxVx, 10AX022xxxxxxxVx, 10AX016xxxxxxxVx, 10AS032xxxxxxxVx, 10AS027xxxxxxxVx, 10AX032xxxxxxxVx, 10AX027xxxxxxxVx, 10AS048xxxxxxxVx, 10AS048xxxxxxxVx
- Fixed a bug that prevented the voltage setting `VCC_ONE = 3.3V` for Intel MAX 10 devices.

Advanced Link Analyzer (formerly JNEye)

- Made the following updates:
  - Updated COM template for CEI-56G-LR/MR-PAM4
  - Fixed Pattern Designer simulation crash bug
  - Fixed IBIS-AMI statistical mode impulse response bug
  - Fixed TX SNDR calculation bug

2.3 IP and IP Cores

Unless stated otherwise, the following IP issues apply to both the Intel Quartus Prime Standard Edition software and the Intel Quartus Prime Pro Edition software.

100G Ethernet IP Core

- Fixed an issue in the Soft 100G Ethernet Core for Intel Stratix 10 devices where, under certain conditions, the PHY would not lock to incoming data.
- Added resiliency to the Rx-PCS lock state. The PCS now checks if the acquired alignment is correct before announcing its lock state, thereby immunizing itself from false-locks and any corruption of initial data

  The PCS does partial decoding of incoming alignment marker bits to optimize logic. This led to a possibility of aliasing and subsequently false locks in some rare cases. To account for this, PCS has a built-in mechanism to recover from the false state and reacquire the lock. However, the sequence implies that in case of a false-lock and immediate start of transmit data, there could be some initial loss of data as PCS self-recovery takes place.
- For Intel Stratix 10 devices, added a fix needed to make RS-FEC work properly in simulation and hardware tests. Also, improved timing margin.
- Fixed SDC constraints for the RS-FEC variant.
- For Intel Stratix 10 devices, updated Low Latency 100G Ethernet IP to support Link Fault, 322Mhz, short packet filtering features. Also, fixeed an issue with FEC.
- Updated the Data Sheet link in the parameter editor to link to *Stratix 10 100G Ethernet IP Core User Guide*.
- Fixed an problem with alignment marker checking in RX-PCS. Before this fix, the check missed checking alignment markers in one clock cycle over an alignment duration of 89k cycles. Because of the missed check, whenever any of the 20 periodic incoming alignment markers aligned with the dead cycle, the logic would get trapped in endless loops of alignment lock/unlock and failed to get a PCS lock.
- Updated example design packet client to improve MAC loopback timing and fix packet a generator size-field bug.

25G Ethernet IP Core

- Improved timing for the RS-FEC variant.
- Enabled multiple profile for Native PHY IP instances when 10/25G mode is enabled.
- Improved IEEE 1588 Precision Time Protocol timing.
- Enabled 10/25G sequencer using `.mif` files
- Enabled 10/25G with RS-FEC.
- Extended rx_bitslip signal because it is an SSR signal.
- Enabled 10/25G IEEE 1588 Precision Time Protocol.
- Disabled multi-profile for Native PHY IP instances.
- Blocked unsupported ED from `hw_tcl` script.
- Improved timing.
- Fixed an NCSIM simulation error.
- Fixed an issue in 10/25G mode without ADME enabled.

- Disabled `khz_ref_clk`register due to timing limitation in devices.
- Improved PTP timing.
- Fixed an issue where 25G RS-FEC DUT is not able to lock after reset.

40G Ethernet IP Core

- Fixed a known simulation issue where the signal `tx_digitalreset` starts up as X, which propagates to the rest of TX PCS logic.
- Enhanced the design example packet generator to allow testing of various packet sizes.
- Fixed the example design generation flow to target the proper device used on the Stratix 10 Signal Integrity Development kit.
- Fixed an issue where bit `0` of `l2_txstatus_error` was unused but was toggling in simulation.

Advanced SEU Detection IP Core

- Added support for Intel Stratix 10 devices.

Arria 10 FPLL IP Core

- Corrected an issue with the FPLL IP when setting counter values manually in core mode.

Clock Control Block IP Core

- For Intel Stratix 10 devices, updated name of the enable input mode on the Clock Control IP from "Falling Edge" to "Negative Latch"'.

DisplayPort IP Core

- Enabled DisplayPort design example on Intel Cyclone 10 devices.
- For Intel Cyclone 10 devices, added design example support for Bitec FMC Daughter Card Rev10 board.
- Fixed DisplayPort AUX channel to handle invalid command and payload length condition.
- Enhanced eDP 1.4 TX to interoperate with eDP 1.4 Sink that support intermediate link rate defined in eDP specification section *Link Rate Discovery and Selection*.
- Enabled DisplayPort AUX channel to handle invalid command and payload length condition.

External Memory Interface IP Core

- Added an update for Intel Arria 10EMIF and Intel Stratix 10 EMIF to ensure a correct write latency value is used when running QDRIV simulations with the Abstract PHY enabled .
- For Intel Stratix 10 EMIF IP, improved timing and hardware robustness.
- For Intel Stratix 10 EMIF IP, improved robustness of DDR4 LRDIMM at 1.3 GHz.

Fractional Phase-Locked Loop (fPLL) IP Core

- Corrected an issue with the fPLL IP when using HDMI protocol in transceiver mode.
- Fixed an issue in the fPLL IP Core QSYS GUI where if you switched from Core mode to another mode, manually modified the L counter value, and then switched back to Core mode, the L counter value might be invalid. The L counter value is now always valid in Core mode.
- Corrected an issue with the Intel Stratix 10 fPLL IP when used in transceiver fractional mode.

HDMI IP Core

- Enabled new selection in the FPLL protocol_mode for HDMI, which allows the FPLL to be configured for input `refclk` down to 25Mhz.
- For Intel Arria 10 devices, optimized the example design to reduce the clock resource by changing the `i2c_clk` to 100Mhz

High Speed Serial Interface (HSSI) IP Core

- Added rules to support Ethernet 25G with AIB FIFO in phase comp mode.
- Enabled the use of remaining eight channels driving by fPLL using xN line when you use all 16 GT channels.
- Reset Controller IP default presets now include Intel Cyclone 10 GX in the name. Previously, the default presets mentioned only Intel Arria 10.
- Fixed internal error related to power virtual attributes and moved those attributes to correct level.
- Added rules to support Ethernet 25G with AIB FIFO in phase comp mode.
- Updated critical warning 19269 with new data rate limits and devices.
- Fixed Intel Arria 10 Transceiver RX PCS control signals when Native PHY IP is configured as non-PCIe Duplex mode with TX PMA+PCS bonding selected.

Integer Arithmetic IP Cores

- Fixed an issue that caused an error when generating LPM_MULT IP core for implementation with logic elements.

Intel Cyclone 10 GX Transceiver PHY IP Core

- Added option to enable the `tx_pma_elecidle` port in **TX PMA Optional Ports** IP core. This port is useful to support protocols such as USB3.1 and SATA.

Intel FPGA Modular ADC (Analog-to-Digital Converter) IP core

- For Intel MAX 10 devices, added a fix to the ADC controller to ensure correct channel select setting during power up sequence. This fix is needed for ADC to correctly switch to temperature sensing mode.

Intel Stratix 10 10GBASE-KR PHY IP Core

- Fixed 10GKR link training CSR reporting false link-training-failed status on hardware test in some seeds.
- Added XCVR Bank voltage selection option to GUI.
- Fixed an interoperability issue.

Intel Stratix 10 PCIe Hard IP Core

- Implemented a fix to ensure that the `hip_mode` value is set correctly for AVMM2. This setting is required for proper DPRIO access to PCIe hare IP.

Interlaken IP Core

- Fixed an issue where you are presented with an invalid board selection for example design with development kits.
- Updated the default scrambler seed for Interlaken (2nd generation) IP and also fixed intermittent CRC32 error in example design hardware.
- Enabled ED hardware for 100G 12x12g variant.

JESD204B IP Core

- Removed the **Target Development Kit** option from **Example Design** tab. The generated design example does not contain pin assignments. You must set up the pin assignments by referring to the targeted board schematic.

Low Latency (LL) Ethernet 10GbE MAC IP Core

- Enabled 10GBASE-R register mode in the GUI.
- Improved timing performance.
- Fixed missing file in `system_console` script.
- Fixed compilation failure when 1.1V analog voltage is selected.

IP for Multi-Rate Ethernet PHY function (formerly 1G/2.5G/5G/10G Multi-Rate Ethernet PHY MegaCore Function)

- Fixed the following Multi Rate PHY design examples for Intel Arria 10 and Intel Stratix 10 devices due to unassigned input pins:
  - 1G/2.5G Ethernet withIEEE 1588 Precision Time Protocol
  - 1G/2.5G/10G Ethernet

Modular Scatter-Gather Direct Memory Access (DMA) IP Core

- Fixed the write master sink command ready so that `snk_commnand_ready` goes high only when the write master response transfer completes. This fix prevents an issue where the data issued from the write master response port is incorrect when back pressure is applied to the write master response port.

Native PHY IP Core

- Fixed an issue where `alt_xcvr_native_helper_functions_*.tcl` worked only with instance names containing single digits in square brackets ("[9]" and below) if you used a naming scheme including square brackets with a number inside. It now works for IP generated instance names containing "[10]" and higher.
- Fixed an issue for some Native PHY IP instances using the multiprofile feature where the transfer clock frequency of one profile was also saved to all other profiles leading to incorrect frequency calculations. This situation occured because the transfer clock frequency parameter sourced from Native PHY IP is a locally derived (that is, calculated from other parameters, not set by the you).

PCIe IP Core

- Fixed an issue where when address mapping is enabled for the Bursting Avalon-MM Slave (aka HPTXS) interfaces, the address was incorrectly mapped for the first TLP generated for the first access to an address mapping window.
- Added last state to LTSSM state display in system console, also changed time value units from number of clock cycle to nanoseconds (ns).

  The PCIe link inspector LTSSM TCL script reads LTSSM states from FIFO. The last state is not stored in FIFO before a LTSSM change.
- For Intel Stratix 10 devices, fixed read failures to other RXM BARs when RXM_BAR0 is not enabled.
- For Intel Stratix 10 devices, fixed an issue with ARI.
- Corrected setting for Intel Stratix 10 L-Tiles and C2P RevA that caused a failure in hardware test.
- Removed the `0bit` option and fixed the `1bit` option to prevent compilation errors when setting the HPTXS mapping parameter.
- Fixed issues that occurred in the Bursting Slave when the lower 4 DWORDs were disabled by deasserting the corresponding bits in the `hptxs_byteenable` bus during the first cycle of a burst write transaction.
- For Intel Arria 10 devices, added PCIe RP IP.
- Fixed an issue preventing the interoperability of the decision feedback equalization (DFE) controller IP and PCIe IP cores.
- Fixed an issue required by the 64-bit Avalon® Memory-Master interface bridge

RAM IP Core

- For Intel Stratix 10 devices, fixed an issue that might cause incorrect operation when a logical memory is implemented with multiple physical memory blocks.

Remote Update IP Core

- (Standard only) Added MT25QL* and MT25QU* flashes.

Serial Data Interface (SDI) IP Core

- Added initial support for Intel Cyclone 10 GX devices.
- for Intel Cyclone 10 GX devices, added support for multirate parallel loopback with VCXO and serial loopback with dynamic clock Tx clock switching hardware in the design example.
- Fixed the following warning generated during PHY IP:

```
The value of parameter pma_txpath_chnsequencer_txpath_chnseq_stage_select
cannot be automatically resolved
```

- For Intel Arria 10 devices, fixed the simulation script by updating the native PHY generated directory path.

SerialLite III Streaming IP Core

- Disabled ECC error when FIFOs are empty. When FIFOs are empty, data from FIFO is expected to be invalid as would the corresponding ECC error.

User Flash Memory IP Core

- (Standard) Added support for Intel MAX 10 10M02SCU324 devices.

Video and Image Processing Suite IP Cores

- Fixed an issue where Deinterlacer II IP configured with Video over film mode synthesizes with a high ALM count and produces multiple warnings about unmatched SDC constraints.
- Introduced additional pipelining to control signals to enable the CVO to close timing to 300 Mhz on some lower speed grade Intel Arria 10 device families. The change of resource utilization is within seed variation.
- Fixed a recovery time violation error in CVI II.

XAUI PHY IP Core

- Fixed incorrect version number.

2.4 Intel FPGA Soc Embedded Development Suite (17.1UP1 RN)

Unless stated otherwise, the following Intel FPGA Soc Embedded Development Suite issues apply to both the Intel Quartus Prime Standard Edition software and the Intel Quartus Prime Pro Edition software.

- Fixed functional failure issues with previous releases that did not show up as configuration issues.

2.5 DSP Builder for Intel FPGAs

Unless stated otherwise, the following DSP Builder for Intel FPGAs issues apply to both the Intel Quartus Prime Standard Edition software and the Intel Quartus Prime Pro Edition software.

- In the V17.1 release, some DSP Builder designs experience a 10-15% reduction in Simulink simulation speeds, relative to V17.0, when automatic testbench (ATB) generation is enabled. The reduced simulation speed is due to an inefficiency in the V17.1 code that writes the ATB stimulus data to the stimulus file. The ATB generation code has been optimized in V17.1 Update 1 and returns simulation speed to parity with 17.0.

  Simulink simulation speed is always lower when ATB generation is enabled and so turn off ATB generation when not required. ATB generation is controlled via the Testbenches tab of the Control block.
- Corrected a bug in the bit-accurate simulation model for the routing registers associated with an Intel Stratix 10 DSP block.

  The effect of this bug is to give incorrect Simulink simulation results for some Intel Stratix 10 models.

  The bug is triggered only when the "bit accurate" option is selected on the SynthesisInfo block for a scheduled subsystem.

2.6 Intel High Level Synthesis Compiler (17.1UP1 RN)

Unless stated otherwise, the following Intel HLS Compiler issues apply to both the Intel Quartus Prime Standard Edition software and the Intel Quartus Prime Pro Edition software.

- Removed restriction on slave memory argument size.
- Fixed an issue that caused incorrect results from `ac_int` multiplication on Microsoft* Windows* systems.
- Improved overall resource estimate accuracy in **Area estimate** high-level design report (`report.html`), especially for designs that use many math functions.
- Added a new tutorial to demonstrate the impact of changing your component interface while keeping the component algorithm unchanged.
- Fixed an HLS header file warning when using the `-Wconversion` compile flag.
- Fixed a compiler crash that would occur when a predicated assignment is used with a zero initializer for a non-integer type.
- Improved the compilation time for certain HLS designs, such as designs with very deep feed-forward datapaths.
- Fixed functional incorrectness in the x86 implementation of the Intel HLS Compiler `ac_int` datatype bit select operation (`slc`).
- Fixed the simulation enqueue behavior of HLS components with slave arguments to prevent a possible hang and provide more efficient execution of the component in simulation.

- Enabled the compilation of components with unused `struct` component arguments.
- (Standard Edition only) For Arria V, Cyclone V, and Intel MAX 10 devices, fixed an issue that might cause incorrect data to be read by a fixed latency Avalon Memory Mapped (Avalon-MM) Master interface.
- (Pro Edition only) Added a random number generator source library (`rand_lib.h`).

2.7 Intel FPGA SDK for OpenCL

Unless stated otherwise, the following Intel FPGA SDK for OpenCL™ issues apply to both the Intel Quartus Prime Standard Edition software and the Intel Quartus Prime Pro Edition software.

- Added `Command has been deprecated` warning message when you use deprecated command options.
- Improved overall resource estimate accuracy in **Area estimate** high-level design report (`report.html`), especially for designs that use many math functions.
- Added the `AOCL_INSTALLED_PACKAGES_ROOT` environment variable so that you can set the path where the `installed_packages` file is created. You can use this environment variable to avoid installing BSPs into the Intel FPGA SDK for OpenCL SDK root directory.
- Modified the OpenCL compiler to allow OpenCL kernels that have a variable named `metadata` to compile. Previously, these kernels caused the OpenCL compiler to terminate with an assert.
- Libkernel DLLs are cleaned up from `/tmp` directory after emulation runs.
- Fixed synchronization of parent and subbuffers between kernel executions.
- Fixed the OpenCL pipes being broken. Removed the hard limit on the number of channels in the emulator. Fixed the host pipes support for emulation.
- Added support for Microsoft* Visual Studio 2015.
- Fixed printing issues in the `aoc` compiler driver.
- Added memory migration support to the profiler when recording memory transfers.
- Prevented hangs on Host Pipes by nudging the device operation queue forward.
- Fixed potential race condition between memory buffer and host pipe operations.
- Fixed an issue where channel depths were sometimes reported incorrectly in the high level design reports (`report.html`). This issue also resulted in incorrect resource estimates being reported for channels.
- Updated Host Pipe APIs to significantly improve bandwidth and latency in the case of parallel invocation in multithreaded host programs.
- Fixed profiler display bug pertaining to invalid values.
- Grouped invalid data warnings in the Profiler.
- Updated OpenCL Profiler to works when multiple channel call sites are used.
- Fixed port naming bug for channel variables in the form of C arrays.

- Fixed compiler crash when multiple read/write accesses to the same channel exist in different kernels. The compiler now generates an error message for this situation.
- Reduced compiler system memory usage.
- Added warning message to the `aoc` command to indicate that you must not share the directory defined by `AOCL_TMP_DIR` across different operating systems. That is, you cannot copy the content of the directory defined by `AOCL_TMP_DIR` from one operating system to the directory defined by `AOCL_TMP_DIR` on a different operating system. Also, you cannot use the same network directory as the same value for `AOCL_TMP_DIR` on different operating systems.
- Updated Intel Arria 10 OpenCL BSP.
- Fixed a potential runtime hang when you have multiple devices installed.
- Added online help links to high level design report (`report.html`).
- Fixed an issue where the `aocl install` command failed with message similar to the following example:

  ```
  is not an object at <path_to_command.pm>/Command.pm line 1241, <F> line 68.
  ```

- Added support for multiple autorun kernel profile captures to the Profiler.
- Fixed an OpenCL compiler crash that could occur when reading or writing to a channel in a loop in a kernel with a barrier and without a `reqd_work_group_size` attribute.

3 Software Issues Resolved

Table 1. Customer Service Requests Resolved in Intel Quartus Prime Design Suite Version 17.1 Update 1

Customer Service Request Numbers Resolved					
11302273	11311829	11312338	11315968	11331355	11342461
11344330	11345455	11347043	11348209	11350039	11351983
11353147	11353226	11353457	11353516	11353597	11353626
11353751	11354254	11354602	11356534	11357012	11360307
11361278					

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4 Software Patches Included in Update Releases

Table 2. Intel Quartus Prime Pro Edition Software Patches included in Intel Quartus Prime Design Suite Version 17.1 Update 1

Software Version	Patch	Customer Service Request Number
Intel Quartus Prime 17.1	0.18	-
Intel Quartus Prime 17.1	0.17	-
Intel Quartus Prime 17.1	0.16	11355064
Intel Quartus Prime 17.1	0.15	-
Intel Quartus Prime 17.1	0.13	-
Intel Quartus Prime 17.1	0.11	-
Intel Quartus Prime 17.1	0.08	11353516
Intel Quartus Prime 17.1	0.06	11351983
Intel Quartus Prime 17.1	0.05b	-
Intel Quartus Prime 17.1	0.04r	-
Intel Quartus Prime 17.1	0.01	-
Intel Quartus Prime 17.0	0.18	11357689

Table 3. Intel Quartus Prime Standard Edition Software Patches included in Intel Quartus Prime Design Suite Version 17.1 Update 1

Software Version	Patch	Customer Service Request Number
Intel Quartus Prime 17.0.2	2.08std	11260252
Intel Quartus Prime 17.0.1	1.03std	11353552
Intel Quartus Prime 16.1	0.28	11334063
Intel Quartus Prime 16.0.2	2.37	11343403

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5 Known Issues and Workarounds

Unless otherwise noted, the following issues affect both Intel Quartus Prime Pro Edition Version 17.1 Update 1 and Intel Quartus Prime Standard Edition Version 17.1 Update 1.

Table 4.

Description	Workaround
(Pro Edition) For Intel Stratix 10 devices, only the following configurations for IOPLL cascading are supported: • IOPLL-IOPLL via dedicated path • IOPLL-IOPLL via core clock Other configurations, such as FPLL to/from IOLL, are not supported. Intel Quartus Prime does not provide a check that disables all cascading between IOPLLs and other types of PLLs, so you can potentially use some unsupported designs.	No workaround is available. Review your designs carefully to ensure that you use only supported configurations for IOPLL cascading.

For information about other known software issues, visit the Intel FPGA Knowledge Base.

Related Links

- Intel FPGA Knowledge Database
- Intel FPGA Documentation: Release Notes
- Intel Quartus Prime and Quartus II Software Support

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Document Revision History

Date	Document Version	Changes
December 2017	2017.12.22	• Initial release with Intel Quartus Prime Design Suite version 17.1 update 1 information.

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