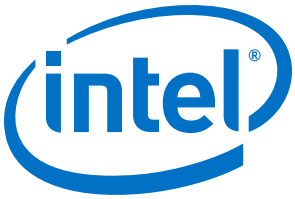

Intel® Quartus® Prime Design Suite Update Release Notes

RN-01080-17.0.2.0
2017.07.28


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Contents

1 Intel® Quartus Prime Design Suite® Version 17.0 Update Release Notes

The *Intel® Quartus® Prime Design Suite Update Release Notes* describe the contents of Intel Quartus Prime Design Suite Version 17.0 software update 2.

Intel Quartus Prime Design Suite updates are cumulative. Update 2 includes update 1.

Intel Quartus Prime Design Suite software updates require Version 17.0 of one of the following software packages:

- Intel Quartus Prime Pro Edition
- Intel Quartus Prime Standard Edition
- Intel Quartus Prime Lite Edition

You must have one of these editions of Intel Quartus Prime software installed before you can install the software updates.

If you use Intel Quartus Prime Lite Edition software, apply the Intel Quartus Prime Standard Edition software update. The Intel Quartus Prime Standard Edition software issues addressed in this update also apply to the device families that are supported by Intel Quartus Prime Lite Edition software.

Related Links

- Intel Quartus Prime Standard Edition Software and Device Support Release Notes Version 17.0
- Intel Quartus Prime Pro Edition Software and Device Support Release Notes Version 17.0

2 Issues Addressed in Update 1

2.1 Intel Quartus Prime Standard Edition Software

Intel Quartus Prime Software GUI

- Corrected an issue where the Tasks panel sometimes incorrectly displayed all processes in a compilation with a question mark next to them, despite the processes running successfully.

Intel Quartus Prime Device Support

- For Intel Arria® 10 devices, enabled missing timing arcs for the HPS NAND interface to the FPGA.
- For Intel Arria 10 devices, updated timing models for Intel Arria 10 devices that support 125 degree operation.

Intel Quartus Prime Compilation and Design Flows

- Fixed an issue in Chip Planner where performing location assignment to a node with a name that contains "\\" did not produce a correct location assignment because the "\\" was omitted and the node could not be identified.
- Fixed an internal error that occurred when trying to assign a differential I/O standard to a node or bus signal that has a name shorter than 2 characters.
- Updated the RTL simulation for specific INI protected use case where LVDS Rx DPA is dynamically reconfigured for specific data bit rates that are lower than PLL minimum frequency.

Fitter

- Fixed an internal error during the fitter when fPLL `c_counter` settings are legal (between 1 and 3) but the fitter still errored out.
- For Intel Arria 10 devices, the RX bonded check was enhanced so that RX-only PCS-bonded designs pass the fitter checks.
- For Intel MAX® 10 devices, fixed an issue where selecting a combination of I/O standard and strength for a Intel MAX 10 device causes an error.

2.2 Intel Quartus Prime Pro Edition Software

Intel Quartus Prime Software GUI

- Fixed a bug in the Qsys GUI where if you change your focus to a subsystem and generate the system, the parent system is skipped.

Intel Quartus Prime Device Support

- Updated packages for the following Intel Cyclone® 10 device models to go from 4 HSSI channels to 6 HSSI channels so that the PCIe Hard IP Core is accessible:
  - 10CX105 (U484 package)
  - 10CX085 (U484, F672 package)

Intel Quartus Prime Compilation and Design Flows

- Improved run time on Windows platforms.
- Fixed the following error that can be caused when Synopsys Design Constraint (.sdc) files in a project include `.` or `..` in an otherwise absolute file path (for example, `/home/me/designs/./project_files/../timing/test.sdc`)

```
Internal Error: Sub-system: QHD, File:
/quartus/comp/qhd/qhd_sdc_database_model.cpp, Line: 143
is_normalized_path(abs_path, m_is_windows)
```

  This fix allows the affected style of path name to be used for SDC files.
- For Intel Arria 10 devices, added a fix to automatically legalize a transceiver setting in a design. The update is applied during the design database import flow. This updated flow enables you to keep your fitter result from a previously compiled design. You must regenerate your bit-streams using the Intel Quartus Prime assembler.
- Fixed an issue in Chip Planner where performing location assignment to a node with a name that contains "\\" did not produce a correct location assignment because the "\\" was omitted and the node could not be identified.
- Fixed an issue with the handling of entity-bound Synopsy design constraint (`.sdc`) files and Windows junction point type file system links.
- Fixed an `undefined entity` error that occured when preserving periphery logic in a `root_partition.qdb` if the original project includes HSSI IP in a default `auto_fab_0` partition. This fix improves the stability of importing periphery logic with a `root_partition.qdb`.

Fitter

- For Intel Arria 10 devices, fixed an issue where the fitter would read the constraints database for Intel Cyclone 10 GX devices instead, causing unforeseen issues such as incorrect bit settings due to different rules-based configuration (RBC) rules between the two device families.
- Fixed an issue that could cause the following Internal Error, when arithmetic output crosses partition boundary:

```
Internal Error: Sub-system: U2B2_CDB, File:
/quartus/db/u2b2/u2b2_cdb_nf_lab_ibr_module.cpp, Line: 342
```

- For Intel Arria 10 devices, removed an unnecessary timing constraint on some clock nets. This change restored the behavior to that seen in Intel Quartus Prime Version 16.1 and earlier. This change is strictly a timing improvement over Intel Quartus Prime Version 17.0.
- For Intel Arria 10 devices, the RX bonded check was enhanced so that RX-only PCS-bonded designs pass the fitter checks.
- Fixed an internal error during the fitter when fPLL `c_counter` settings are legal (between 1 and 3) but the fitter still errored out.

2.3 IP and IP Cores

Unless stated otherwise, the following IP issues apply to both the Intel Quartus Prime Standard Edition software and the Intel Quartus Prime Pro Edition software.

DisplayPort IP Core

- Refined DisplayPort TX PMA settings based on compliance testing to enable optimized transceiver performance.
- Fixed inaccurate transmission of MVID value at certain boundary values. This issue caused the pixel clock generation on the corresponding DisplayPort sink to be potentially wrong.
- Enhanced the DisplayPort RX API to handle the scenario where the GPU produces a one-time burst of bit errors after link training completes.

Low Latency (LL) Ethernet 10GbE MAC IP Core

- For Intel Quartus Prime Pro Edition software running on Windows platforms, fixed the Intel Arria 10 example design generation errors.

External Memory Interface IP Core

- Removed a default timing constraint that was applied to the `altera_reserved_tck` clock, which is used for ISSPs and SLD tools. You must add the proper timing constraint for this design based on your JTAG topology in `jtag_example.sdc`.

Fractional Phase-Locked Loop (fPLL) IP Core

- For Intel Arria 10 devices, restricted the use of the 25 Mhz reference clock for fPLL to the HDMI protocol. This restriction also returns the minimum reference clock for fPLL in core mode to 27MHz.

HDMI IP Core

- Resolved possible HDMI design example IP generation issue in Windows systems caused by the Java script character limit being exceeded.
- Updated the HDMI RX IP core to fix timing violation that occurred when you connected each input `ls_clk` to independent clocks. This violation caused the channel data paths to be asynchronous after lane deskewing and alignment.
- Updated design example to work around interoperability issues with certain HDMI sources. Switching between different color space using certain HDMI source might cause no display or image distortion on the HDMI sink. This problems is caused by the following issues that have been corrected:
  - Read requests from the auxiliary bypass FIFO have a problem that caused missing end-of-packets in the last auxiliary packet.
  - Because the HDMI reconfiguration state machine performs a reconfiguration when the CD[3:2] from General Control Packet is `2'b01`. According to HDMI 1.4b specification, video with 24 bit per pixel can be indicated as CD[3:0] is `4'b0100`. However, certain source considers 24 bits per pixel as non-deep color ("Color Depth not indicated") and then transmits CD[3:0] as `4'b0000`. This transmission affects existing reconfiguration logic which monitors where CD[3:2] to trigger reconfiguration required for deep color.

I/O Phase-Locked Loop (IOPLL) IP Core

- For Intel Cyclone 10 GX devices, addressed an issue where IOPLL IP cores did not generate correctly.

JESD204B IP Core

- For Intel Arria 10 devices, fixed the following issues related to the transceiver dynamic reconfiguration interface:
  - The reconfig_* ports are unconnected in ED for L=1.
  - VHDL reconfig_* port type mismatch (std_logic, std_logic_vector).
  - Unconstraint reconfig_clk in standalone IP.
  - Unconnected reconfig_* ports in IP simulation.

Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core

PCIe Hard IP Core

- For Intel Arria 10 devices, made the following updates
  - Enabled a hardware cap value of 10.
  - Fixed a bug in Intel Quartus Prime for mapping a hard IP atom parameter.
  - Updated the PCIe hard IP to use a consistent value for the HIP parameter across all revisions.
- For V-Series Avalon-MM DMA Interface, the ByteEnable signal is now visible in 128-bit mode.
- For Intel Arria 10 devices, resolved the ModelsSim VHDL compile error.

RapidIO IP Core

- Fixed an issue where the next expected acknowledge packet ackID does not increment when triggering the bit-23 PORT_DIS of Port 0 Control CSR.
- Fixed an issue where spurious packets are sent after link partner re-initializes from reset.
- Fixed an issue where the outbound/transmitted packet ackID is out of sync after link partner re-initializes from reset.
- Fixed an issue where Port OK does not assert occasionally when resetting the link partner.

Serial Data Interface (SDI) IP Core

- Fixed a VHDL compilation issue in the NCSim simulator.

SerialLite III Streaming IP Core

- Fixed the SerialLite III VHDL example design which fails in the `ncsim` command due to an NC Sim version update.

Transceiver PHY IP Core

- Added a fix to handle the incorrect behavior of CDR controller and signal detect block for Electrical Idle entry in Gen2 and Gen3 in PCIe bonded designs.
- For Arria 10 devices, removed the following warning:

```
The value of parameter hssi_common_pcs_pma_interface_bypass_pma_sw_done"
cannot be automatically resolved.
Valid values are: true false.
```

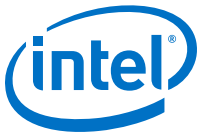
Video and Image Processing Suite IP Cores

- Enabled Intel FPGA IP Evaluation Mode (formerly OpenCore Plus) evaluation for the configurable guard bands IP core.
- Fixed Video IP simulation models compilation issues in VCS/NCSIM.
- Fixed a bug where the Deinterlacer II IP core does not function correctly when configured in motion adaptive mode high quality mode but without video-over-film cadence correction.

2.4 Intel FPGA SDK for OpenCL

Unless stated otherwise, the following Intel FPGA SDK for OpenCL™ issues apply to both the Intel Quartus Prime Standard Edition software and the Intel Quartus Prime Pro Edition software.

- Updated fast-compile settings to remove LU decomposition limit and static timing analysis (STA) calls.
- For Intel Arria 10 SX devices, connected HPS IP reset ports to fix base and flat compile.
- Updated the `cl_ext.h` with modified define values to avoid conflicts with the emulator.
- Fixed the problem with using `vstore_halfn` and `vstore_half` compiled for the emulator.



- Fixed bug in handling of constant arrays.
- Fixed a bug which causes problems in the `aoc` compiler when you specify absolute paths for the project directory.
- Fixed an issue that caused the following assertion:

  ```
  acl_thread.h:47:acl_sig_started: Assertion '!acl_inside_sig' failed
  ```

- Fixed a situation where the compiler deletes a project directory even when it was not originally created by the compiler. The first time that you compile a project with the updated version of the compile, you might need to delete the old project directory manually.
- On Windows systems, the compiler now exposes Intel Quartus Prime errors to `stdout` and warns you that missing file errors might be caused by file name length limits.
- For Intel Arria 10 GX devices, added support for the Ubuntu Version 16.04 operating system.
- This fix correctly sets up the path to the required Qsys tools for the Intel FPGA SDK for OpenCL Offline Compiler targeting Arria 10 based board support packages. Without this fix, the compiler fails in the ip-generate stage and outputs a `sh: qsys-archive: command not found` message to the log file.

3 Issues Addressed in Update 2

3.1 Intel Quartus Prime Standard Edition Software

Intel Quartus Prime Installation

- Fixed an issue that caused the 32-bit Intel Quartus Prime Programmer and tools package to be missing from Intel Quartus Prime Standard Edition Version 17.0.

Intel Quartus Prime Software GUI

- Fixed a problem where no message is prompted when the Intel Quartus Prime Block Editor failed to launch MegaWizard plug-in manager because the IP component could not be found in the specified library paths.
- For Intel Arria 10 devices, fixed an issue preventing users from archiving `.qpf` and `.qsf` files in advanced archive mode.

Intel Quartus Prime Device Support

- Fixed an issue where the baseline pinouts provided with Intel Quartus Prime software were for a previous version.
- Fixed an issue that could cause Qsys to assign an incorrect clock frequency for the hard processor system (HPS) IP component when using certain Cyclone V SoC devices.
- Fixed an issue that caused the Nios® II Software Build Tools to not support Intel Cyclone 10 LP devices in Intel Quartus Prime Version 17.0.
- Updated the Intel Quartus Prime device database to increase the number of HSSI channels from 4 to 6 for the following Intel Cyclone 10 devices so that the PCIe hard IP core is accessible:
  - 10CX105 (U484 package)
  - 10CX085 (U484, F672 package)

Intel Quartus Prime Compilation and Design Flows

- Fixed the following Qsys error that occurred if there was a significant access time delay in accessing the device database from the Intel Quartus Prime Standard Edition installation directory when Qsys is loading:

```
Can't initialize DevFamilyManagerFromDB
```

- Enhanced SSH support in Design Space Explorer (DSE) II by supporting port forwarding to allow a remote host that is separated by a firewall to connect to the DSE server using localhost.
- Fixed an error where DSE II exited with a non-zero error code when you used the `--stop-after-timing-met on` option despite one of the seeds meeting timing. DSE now exits with a success error code if one of the seeds meets timing when you use the `--stop-after-timing-met on` option.
- Provided new environment variables so that you can specify separate compile options for Verilog and VHDL. You can use the following environment variables in addition to `USER_DEFINED_COMPILE_OPTIONS` to specify compile options:
  - `USER_DEFINED_VERILOG_COMPILE_OPTIONS`
  - `USER_DEFINDE_VHDL_COMPILE_OPTIONS`
- For Arria 10 devices, added a fix to automatically legalize a transceiver setting in a design. The update is applied during the design database import flow. This updated flow enables you to keep your fitter result from a previously compiled design. You must regenerate your bit-streams using the Intel Quartus Prime assembler.
- Fixed an issue where the `quartus_syn` command sometimes incorrectly issues the following error message :

```
Can't open project -- you do not have permission to write to all the files or
create new files in the project's database directory
```

- Fixed an issue where, when single event upset (SEU) sensitivity map file (.smh file) generation is enabled in your design, the engineering change order (ECO) netlist change might cause Intel Quartus Prime quit unexpectedly with following error message:

```
Internal Error: Sub-system: FITCC, File: /quartus/fitter/fitcc/
fitcc_asd_utility.cpp, Line: 477
```

Programmer

- Fixed a bug in the `quartus_hps` utility where the last word of bulk reading when reading back flash device data is incorrect.
- For Intel Cyclone 10 LP devices, updated the serial flash loader (SFL) image.

Fitter

- For Arria V industrial grade devices, improved the hold timing closure for paths to DSP blocks.
- On Windows systems, increased the amount of stack memory allocated to the `quartus_fit` command so that the stacks size on Windows systems is the same as on Linux systems.

Intel FPGA University Program

- Updated the following tutorials on the Intel FPGA University Program website at https://www.altera.com/support/training/university/materials-tutorials.html. The tutorials apply only to Intel Quartus Prime Standard Edition:
  - *Quartus Prime Introduction Using Verilog Designs*
  - *Quartus Prime Introduction Using VHDL Designs*
  - *Quartus Prime Introduction to Simulation of Verilog Designs*
  - *Quartus Prime Introduction to Simulation of VHDL Designs*

3.2 Intel Quartus Prime Pro Edition Software

Intel Quartus Prime Documentation

- Fixed an issue that caused an incorrect version of local help files to be included with Intel Quartus Prime Pro Edition Version 17.0 software. The correct version is available as a separate download.

  To update your local copy of the Intel Quartus Prime help files, download **Quartus Prime Pro Edition Help v17.0 Update 2** from the Updates tab for Intel Quartus Prime Pro Edition Version 17.0 at the Intel FPGA Download Center (https://dl.altera.com/) and install the updated help package.

  If you use the online version of the Intel Quartus Prime Pro Edition help, you do not need to install this update.

Intel Quartus Prime Software GUI

- Fixed an issue with the Compilation Dashboard invalidating a compilation status that should still be valid on the open project.

Programmer

- Fixed a bug in the `quartus_hps` utility where the last word of bulk reading when reading back flash device data is incorrect.

3.3 IP and IP Cores

Unless stated otherwise, the following IP and IP core issues apply to both the Intel Quartus Prime Standard Edition software and the Intel Quartus Prime Pro Edition software.

External Memory Interface (EMIF) IP Core

- (Intel Quartus Prime Standard Edition only) For Arria V and Cyclone V devices, ensured that only memory configurations that match the supported DDR3 memory densities can be selected during IP generation for Arria V and Cyclone V hardened memory controllers.
- (Intel Quartus Prime Standard Edition only) For Arria V, Cyclone V, and Stratix® V devices, fixed the EMIF example simulation designs for the DDR2 next-generation controller so that they no longer fail during elaboration due to an unassociated port (AFI_SEQ_BUSY) when using the Synopsys VCSMX or Cadence NCSIM simulators.

High-Definition Multimedia Interface (HDMI) IP Core

- Fixed the Intel Intel Arria 10 HDMI design example to ensure that the HDR InfoFrame is filtered in its entirety from the loopbacked auxiliary data.

  The design example demonstrates High Dynamic Range (HDR) InfoFrame sample data insertion into HDMI TX core and filtering of existing HDR InfoFrame from the loopbacked auxiliary data. The previous design had a flaw that caused the Start-of-Packet of the HDR InfoFrame to be preserved, while the other HDR data content and End-of-Packet are filtered correctly.
- Fixed an error in the Intel Intel Arria 10 HDMI design example where the TX PMA recalibration was not triggered after data rate switching. This error might cause occasional hardware failure for data rates greater than 5 Gbps. This fix ensures that TX PMA recalibration is initiated when the data rate changes.
- Fixed an issue where unnecessary critical warnings are reported on `gcp_cd` and `gcp_dd` registers. The warning indicates only a discrepancy between the Intel Quartus Prime default register assignment value and the RTL initialized register value. Because register values are reassigned and valid only upon reset, removing the RTL initialized values help resolves these critical warnings.

JESD204B IP Core

- (Intel Quartus Prime Pro Edition only) For Intel Arria 10 devices, fixed an issue in the example design where you choose to generate a VHDL simulation in the Example Design GUI but the file sets generated are Verilog files.

Partial Reconfiguration IP Core

- (Intel Quartus Prime Standard Edition only) For Stratix V devices, fixed a potential internal error (IE) that is caused by register duplication of `prpof_id_reg`.

PCIe Hard IP Core

- For Intel Arria 10 devices, constrained the `pld_rx_data` paths with stricter rules that make them effective on PCIe IPs only when skip order set detection logic is enabled by the `enable_skp` parameter.
- For Intel Arria 10 devices, fixed an issue causing unconstrained clocks in Timing Analyzer (formerly TimeQuest).

Serial Digital Interface (SDI) II IP Core

- Fixed simulation run script to be compatible with the latest Qsys generated simulation setup script.

Video and Image Processing (VIP) Suite

- Fixed an issue in Clocked Video Output (CVO) II preventing the correct elaboration of Qsys generated VHDL testbenches.
- Fixed a lockup in the Scaler II IP core Nios II driver when computing coefficients.

3.4 Intel FPGA SDK for OpenCL

Unless stated otherwise, the following Intel FPGA SDK for OpenCL issues apply to both the Intel Quartus Prime Standard Edition software and the Intel Quartus Prime Pro Edition software.

- Fixed an error where compiles targeting Intel Arria 10 boards stop responding on shared Linux systems.
- Fixed an issue where the Intel FPGA RTE for OpenCL is missing from Intel Quartus Prime Design Suite® Version 17.0 Update 1.
- Fixed an issue where the `gdb` command printed the wrong local variable values when running the OpenCL emulator.
- Provided a new compile command option that you can use when you encounter challenges correcting Windows long-path errors in your design.

  If you compile a design that causes a Windows long-path error, you can force the compiler to limit the generated path and file name lengths by adding the following option to the HLD compiler command:

  ```
  --llc-arg --set-dspba-
  feature=maxFilenamePrefixLength,integer,<N>,maxFilenameSuffixLength,integer
  ,<M>
  ```

  You can set the values <*N*> and <*M*> to any positive integer value. The default values for <*N*> and <*M*> are `80` and `20`, respectively.

  Lower values for <*N*> and <*M*> result in shorter but less comprehensible file names. Use this command option only when other approaches have failed to solve your long-path issue because this command option can result in obfuscated names that make functional debug difficult.
- Updated the license library to accept older, yet still valid, licenses.
- Fixed issues with the summary reports where the device (acl) static report did not load and inner loop initiation interval (II) was presented with no explanation.
- Improved loop initiation interval (II) on some OpenCL designs by analyzing global memory dependencies more accurately.

4 Software Issues Resolved

Table 1. Customer Service Requests Resolved in Intel Quartus Prime Design Suite Version 17.0 Update 1

Customer Service Request Numbers Resolved					
11266103	11276040	11280782	11281478	11293397	11302641
11302641	11306504	11307454	11311366	11314093	11317825

Table 2. Customer Service Requests Resolved in Intel Quartus Prime Design Suite Version 17.0 Update 2

Customer Service Request Numbers Resolved					
11291205	11307817	11316320	11318925	11320414	11323147
11326902					

5 Software Patches Included in Update Releases

Table 3. Software Patches included in Intel Quartus Prime Design Suite Version 17.0 Update 1

Software Version	Patch	Customer Service Request Number
Intel Quartus Prime 17.0	0.07	11314093
Intel Quartus Prime 17.0	0.03	-
Intel Quartus Prime 16.1.2	2.17	11298413
Quartus II 15.0.2	2.25	11266103

Table 4. Software Patches included in Intel Quartus Prime Design Suite Version 17.0 Update 2

Software Version	Patch	Customer Service Request Number
OpenCL 17.0.1	1.01cl	11316320, 11320414
Intel Quartus Prime 17.0.1	1.02	11318345
Intel Quartus Prime Standard Edition 17.0.1	1.01std	-
Intel Quartus Prime 17.0	0.13	-
Intel Quartus Prime 17.0	0.15	11325092
Intel Quartus Prime Standard Edition 17.0	0.05std	-
Intel Quartus Prime 16.1.2	2.22	11314528
Intel Quartus Prime 16.1.1	1.08	11320432

6 Known Issues and Workarounds

For information about known software issues, visit the Intel FPGA Knowledge Base.

Related Links

- Intel FPGA Knowledge Database
- Intel FPGA Documentation: Release Notes
- Intel Quartus Prime and Quartus II Software Support

Document Revision History

Date	Document Version	Changes
July 2017	2017.07.28	• Adjusted chapter numbers. • Updated product names to reflect Intel trademark requirements • Updated document to contain information about Intel Quartus Prime Design Suite version 17.0 update 2.
June 2017	2017.06.16	• Initial release with Intel Quartus Prime Design Suite version 17.0 update 1 information.