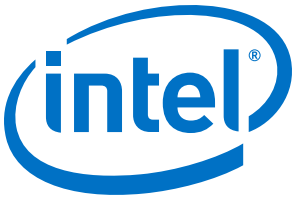


Quartus Prime Design Suite Update Release Notes

RN-01080-16.1.2.0
2017.01.27


Subscribe


Send Feedback

Contents

1 Quartus Prime Design Suite® Version 16.1 Update Release Notes

This version of the *Quartus® Prime Design Suite Update Release Notes* describes the Quartus Prime Design Suite version 16.1 software update 2.

Quartus Prime Design Suite updates are cumulative. Update 2 includes update 1.

The Quartus Prime Design Suite software update requires the Intel® Quartus Prime Standard Edition software release version 16.1 or the Intel Quartus Prime Pro Edition software release version 16.1. If you do not have either edition of the Quartus Prime software release version 16.1, install it prior to installing any Quartus Prime Design Suite version 16.1 software updates to ensure the Quartus Prime software runs properly.

You can apply this software update to the Quartus Prime Lite Edition software, which supports the Arria® II, Cyclone® IV, Cyclone V, MAX® II, MAX V, and MAX 10 FPGA device families. The Quartus Prime Standard Edition software issues that apply to these device families also apply to the Quartus Prime Lite Edition software.

Related Links

- Quartus Prime Standard Edition Software and Device Support Release Notes Version 16.1
- Quartus Prime Pro Edition Software and Device Support Release Notes Version 16.1

1.1 Issues Addressed in Update 1

1.1.1 Quartus Prime Standard Edition Software

1.1.1.1 Quartus Prime Device Support

- Fixed incorrect pinout file for Arria 10 10AX115 devices. Previously when HSSI transceivers are used in Arria 10 10AX115 devices, RREF pins were incorrectly shown as GND.
- For Cyclone IV GX devices, updated the data rate rules-based configuration rule to be 2.5 Gbps. Previously it was 2.4 Gbps.
- Fixed a bug present in the Quartus Prime Standard Edition software versions 16.0 and 16.1 that prevents gate-level timing simulation netlist generation for MAX II and MAX V device families, which support both timing and functional simulation. This fix enables timing simulation support for MAX II and MAX V devices.

1.1.1.2 Quartus Prime Software Installation

- This fix correctly sets up the path to the required Qsys tools within the Quartus installation for the Intel FPGA SDK for OpenCL Offline Compiler targeting Arria 10 based board support packages. Without it, the offline compiler fails in the ip-generate stage and outputs a `sh: qsys-archive: command not found` message to the log file.

1.1.1.3 Quartus Prime Compilation and Design Flows

- Fixed the `-operating_conditions` option for the `set_timing_derate` and `set_annotated_delay` SDC commands. Previously, the commands were being ignored when this option was specified.
- Fixed a memory corruption issue with the Convert Programming Files utility when converting an Arria 10 Partial Reconfiguration bitstream with multiple attempts.
- Fixed an internal error in TimeQuest that might happen when running Macro tasks (Report Top Failing Paths, Report All Core Timings) while empty report panels for those tasks already exist in the Report view.
- Area savings for non-blocking channels.

1.1.1.4 Quartus Prime Programmer

- The `quartus_hps` command is enhanced to support NAND bad block management.

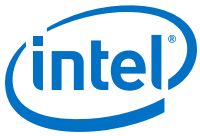
1.1.1.5 Fitter

- Fixed `Error: Can't route signal` for certain clock signals that feed peripheral destinations in the following device families: Arria V, Arria 10, Cyclone V, Cyclone 10, MAX V, MAX 10, and Stratix V.
- For Arria 10 devices, fixed an issue where two registers with shared signals in the same ALM could fail to be clustered.
- Fixed simulation errors of fitting results due to incorrect default input port connections to VCC. This issue affected all device families except Arria 10.
- Improved the routing algorithm to reduce run-time in the presence of excessively large hold constraints.

1.1.2 Quartus Prime Pro Edition Software

1.1.2.1 Quartus Prime Device Support

- Fixed incorrect pinout file for Arria 10 10AX115 devices. Previously when HSSI transceivers are used in Arria 10 10AX115 devices, RREF pins were incorrectly shown as GND.



1.1.2.2 Quartus Prime Software Installation

- This fix correctly sets up the path to the required Qsys tools within the Quartus installation for the Intel FPGA SDK for OpenCL Offline Compiler targeting Arria 10 based board support packages. Without it, the offline compiler fails in the ip-generate stage and outputs a `sh: qsys-archive: command not found` message to the log file.

1.1.2.3 Quartus Prime Compilation and Design Flows

- Fixed the issue where, when migrating a project to Qsys Pro, files failed to be added to project properly when processing a higher number of files.
- Fixed an issue where IP core file paths were being stored as absolute paths instead of relative paths. With this fix, the file paths added to a Quartus project are relative paths.
- Fixed an internal error that can occur when clicking **Project ➤ Clean Project**.
- Fixed a Qsys error `Can't initialize DevFamilyManagerFromDB` when loading Qsys if there was a significant access time delay in loading the device database from Quartus Prime installation directory.
- Fixed a memory corruption issue with the Convert Programming Files utility when converting an Arria 10 Partial Reconfiguration bitstream with multiple attempts.
- Fixed an internal error in TimeQuest that might happen when running Macro tasks (Report Top Failing Paths, Report All Core Timings) while empty report panels for those tasks already exist in the Report view.
- Fixed an error about missing encrypted source files while trying to run Rapid Recompile.
- When running the partial reconfiguration flow script from the Quartus Pro GUI, it might fail with the error: `The Arria 10 PR compile flow script can only be run from the Quartus GUI or quartus_sh.`
- Area savings for non-blocking channels.

1.1.2.4 Quartus Prime Programmer

- The `quartus_hps` command is enhanced to support NAND bad block management.

1.1.2.5 Fitter

- For Arria 10 devices, fixed an issue where two registers with shared signals in the same ALM could fail to be clustered.

1.1.3 IP and IP Cores

Attention: Unless stated otherwise, the following IP issues apply to both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

ASMI Parallel IP Core

- Fixed the quad write opcode (0x12 => 0x38) for EPCQ512.

Color Plane Sequencer IP Core

- In Quartus Prime Pro Edition, fixed a compilation error for the Video IP Color Plane Sequencer II.

Deinterlacer II IP Core

- The Video and Image Processing Suite Deinterlacer II IP core, when configured in "weave" mode, exhibits a bug whereby the Avalon-ST video "end of packet" flag is not being set correctly at the end of video packets. In a system, this manifests as an extra long video packet with no following control packet (as the control packet is interpreted as the completion of the video packet). This bug is fixed in this release.
- Fixed incorrect product ID code.

DisplayPort IP Core

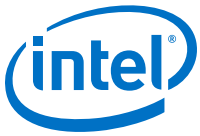
- Updated the IP path in `build_ip.tcl` script to fix the "`cannot find IP path`" error.
- Updated the DisplayPort TX Transceiver Channel Bonding Mode from PMA_Only to PMA_and_PCS Bonding in order to meet the DisplayPort lane-to-lane output skew requirement.
- Updated the Arria 10 Design Example top level and `.qsf` files to clean up most of the warnings.
- Enhanced the DisplayPort Design Example Generation option to remove "None" from SST Design Variant.

External Memory Interface IP Core

- For Arria 10 devices, input terminations below 60 ohms are not supported for the following I/O standards:
  - SSTL-12
  - SSTL-135
  - SSTL-15
  - HSTL-12
  - HSTL-15
- For Arria 10 devices, for RLDRAM3 designs:
  - SSTL-12 is the default I/O standard.
  - For SSTL-12 I/O standard, 34 ohm drive strength for Rs (Output Mode) is enabled.

HDMI IP Core

- Removed the "None" option from design example type selection.
- Fixed HDMI TX data island trailing guardband encoding which otherwise results in incremental errors for channel 1 and 2 reported by an attached sink.
- Fixed HDMI TX ScrmblrCnt initialization logic.
- Removed null packet transmission during data island period to resolve instability issue during HDMI 2.0 operations where dropped frames and incremental error at channel 0 could be significant with certain monitors.



Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Core

- A logic change that was introduced in the 15.1 release of the 40G and 100G Low Latency Ethernet cores can cause a reset loop issue that prevents the RX side from coming up. This occurs only for a small number of compilations, and is a function of the routing delays. This update prevents this problem.

Parallel Flash Loader IP Core

- Enabled Parallel Flash Loader (PFL) II. Fixed compilation error for multiflash. Fixed the issues of halt state cannot be selected. Fixed the issues for not allowing PFL II to trigger reconfiguration when FPGA **conf_done** is high.
- Enhanced PFL to support multidie for Arria 10 developer kit and update the note to reflect FPPx16 and FPPx32 are supported by Arria 10. The note is visible when you select FPPx16 or FPPx32 configuration.

Video and Image Processing Suite IP Cores

- Fixed an issue where interlaced fields were being mislabeled (F0 as F1 and F1 as F0) by the Clocked Video Input II IP core when the `Extract field signal` parameter is enabled.
- This update allows the Video and Image Processing Suite IP cores to more easily achieve 300MHz operation on Arria 10 C2 parts.

1.1.4 JNEye

Attention: Unless stated otherwise, the following JNEye issues are associated with both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

- Made the following updates:
  - Fixed Windows 10 GUI text scaling issue.
  - Fixed IBIS-AMI GUI crash issue when a text box becomes empty during entry.
  - Addressed issue where JNEye cannot import S-parameter in UTF-8 with BOM header.
  - Fixed incorrect repeater/retimer jitter parameter import issue.
- Made the following updates:
  - Fixed COM channel compliance crash issue.
  - Fixed repeater/retimer jitter component type mapping issue.
  - Added Stratix 10 H-tile TX slew rate configuration file.
  - Updated default Stratix 10 H-tile package model.

1.1.5 Intel FPGA SDK for OpenCL

Attention: Unless stated otherwise, the following Intel FPGA SDK for OpenCL™ issues are associated with both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

- Print library creation error message to stderr, not just to log file.
- Fixed a crash caused by certain pattern of accessing memory inside conditional code.
- Fixed a problem in the OpenCL guaranteed timing flow where in some cases small setup timing violations of the kernel clock can be observed due to varying jitter characteristics of the IOPLL at different configurations. The IOPLL is now iteratively adjusted in the OpenCL post-flow script which resides in the OpenCL SDK.
- Fixed the incorrect results of float-to-int rounding modes in emulation.
- Added the option to set the process affinity for emulator with the `CL_CONTEXT_EMULATOR_PROCESS_AFFINITY_MASK_ALTERA` environmental variable.

1.1.6 Intel SoC FPGA Embedded Design Suite

- The `quartus_hps` command programs all the data in the programming file, even the entire page consists entirely of `0xFF` data. Previously, the `quartus_hps` command skipped programming a page of data if the intended programming file data for that page is all `0xFF` values, causing error-correcting code to not be calculated.

1.1.7 DSP Builder for Intel FPGAs

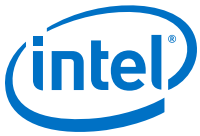
- Fixed problem where the simulation of designs is noticeably much slower when they use ModelBus blocks.

1.2 Issues Addressed in Update 2

1.2.1 Quartus Prime Standard Edition Software

1.2.1.1 Quartus Prime Device Support

- For Arria 10 devices, when Quartus Prime software detects a bad pin during HPS pin placement, Quartus might generate an internal error when creating the error message string. This fix addresses this issue, and the error message indicating that the bad pin placement now displays properly.
- For Arria V GX and Arria V SX devices, updated the default Rx V_{cm} & Rx V_{th} Quartus Prime settings to fix the risk of functional failure for PCIe configuration with the existing Quartus Prime settings.
- For Arria V, Cyclone V, MAX V, and Stratix V devices, enabled IP-migration for `altera_mult_add` from older versions of Quartus Prime to Version 16.1.



1.2.1.2 Quartus Prime Compilation and Design Flows

- Fixed a `Fatal Error: Segment Violation` error when running the `quartus_map` command. The error can occur for a project that contains a **.sdc** file that makes calls to the `get_integer_node_delay` and `get_micro_node_delay` functions.
- Fixed an internal error during IBIS model generation when you enable the **Extended Model Selector** option.
- Reduced read margin due to the non-linearity of PMOS IO transistors included in IO models. This change impacts models of center tap terminated (CTT) IO standards when input termination is enabled. As a result, IBIS models and input buffer delays of such IO configurations are impacted.

1.2.1.3 Quartus Prime Software GUI

- Fixed an issue with the In-System Memory Content Editor that caused it to crash unexpectedly after a few read/write operations.
- Fixed an internal error that occurred when you selected **Project ➤ Archiving Project ➤ Advanced**, and then selected any option other than **Source Control**.
- Updated the Arria 10 documentation links displayed in the Qsys GUI. Also, removed QSF assignments that no longer need to be explicitly specified.

1.2.1.4 Quartus Prime Programmer

- Added a 10 ms delay after the ISC_ENABLE instruction for MAX 10 devices to compensate for engineering delay.
- For Stratix V devices, fixed an issue with Configuration via Protocol (CvP) configuration scheme bitstreams when you have encrypted bitstreams that are uncompressed.
- For MAX 10 devices, fixed an issue with converting a `.ekp` file to a `.jam` file.
- Modified PFL II to support version 5 of the Programmer Object File (POF) format. With POF format version 5, PFL II can send exact data to the device.
- For MAX II and MAX V devices, fixed an issue where real-time ISP programming was not taking effect with `.jbs` and `.jam` files. The ISP clamp is skipped when you enable real-time ISP.
- Fixed a case where an internal error occured under certain conditions during SVF generation.
- Improved programming file generation error message handling.

1.2.1.5 Fitter

- Fixed a class of problems that can occur when Synopsys Design Contstraints (SDC) exceptions expand to a larger set of cells later in fitter. This condition caused an internal error when the system detected that physical synthesis attempted to delete cells with a timing exception.
- For Arria 10 devices, fixed a misleading critical warning where Shared HPS I/O pins were subject to the same check that ensures that the voltage on the HPS-dedicated I/O pins voltage corresponds to the declared VCCIO_HPS setting. The Shared HPS I/O voltage is independent of the VCCIO_HPS setting, and should not be subject to the check. This fix removes the misleading critical warning for the Shared HPS I/O pins.
- Fixed a problem that might occur when two logical DSP blocks are merged to share a single physical DSP location. This problem occured only if all of the following conditions were true:
  - The logical DSP blocks used a precision mode where two logical instances can share a single physical block:
    - Arria V GZ and Stratix V devices: independent mode 18x18 with 32-bit resolution (`mode = "M18X18_PARTIAL"`).
    - Arria V, Arria 10, and Cyclone 10 devices: independent 18x18 (`mode = "M18X18_FULL"`)
  - The logical DSPs were merged into a single physical location. The DSP merge appeared in the Netlist Optimizations report, and the DSP details report showed connected inputs for both the `ay` and `by` input signals.
  - The merge DSP block used the internal coefficient table of the DSP. That is, the **Uses Coefficient** column in the DSP details report shows `yes`, and the the `coefsela` and `coefselb` inputs are connected instead of the `ax` and `bx` inputs.
  - The coefficients stored in the internal table were to be interpreted as signed values.

  Under these circumstances, the multiplication assigned the B half of the physical DSP block incorrectly treated the coefficients as unsigned values, leading to an incorrect result for mulitplication operations involving a negative coefficient value.
- Improved hold timing closure during partial reconfiguration, when a clock is shared between a preserved static design partition and a partial reconfiguration design partition.
- For MAX 10 E114 package devices, ehances the fitter for output to PLL clock input geometry rule. Previously, the fitter was unable to differentiate the PLL input clock from other PLL input ports.

1.2.2 Quartus Prime Pro Edition Software

1.2.2.1 Quartus Prime Device Support

- For Arria 10 devices, when Quartus Prime software detects a bad pin during HPS pin placement, Quartus might generate an internal error when creating the error message string. This fix addresses this issue, and the error message indicating that the bad pin placement now displays properly.

1.2.2.2 Quartus Prime Compilation and Design Flows

- Fixed a `Fatal Error: Segment Violation` error when running the `quartus_map` command. The error can occur for a project that contains a **.sdc** file that makes calls to the `get_integer_node_delay` and `get_micro_node_delay` functions.
- Fixed an internal error during IBIS model generation when you enable the **Extended Model Selector** option.
- Reduced read margin due to the non-linearity of PMOS IO transistors included in IO models. This change impacts models of center tap terminated (CTT) IO standards when input termination is enabled. As a result, IBIS models and input buffer delays of such IO configurations are impacted.
- Fixed a bug in IBIS file generation (with the model selector feature enabled) where the model name of a negative differential pin did not match the model name of its positive pin complement.

  For True Differential output pins, the negative model name might still be different from the positive model name.

  You can correct this issue after Quartus Prime Pro Edition has generated the IBIS file by replacing the negative pin model name with its positive complement pin model name in the IBIS file.

1.2.2.3 Supported EDA Tools

Synopsys Syplify

- The following versions of Quartus Prime Pro Edition support Synopsys Synplify Version 2106.09-SP1:
  - Quartus Prime Pro Edition Version 16.1
  - Quartus Prime Pro Edition Version 16.1 Update 1
  - Quartus Prime Pro Edition Version 16.1 Update 2

1.2.2.4 Quartus Prime Software GUI

- Fixed an issue with the In-System Memory Content Editor that caused it to crash unexpectedly after a few read/write operations.
- Fixed an internal error that occurred when you selected **Project ➤ Archiving Project ➤ Advanced**, and then selected any option other than **Source Control**.

1.2.2.5 Quartus Prime Programmer

- Added a 10 ms delay after the `ISC_ENABLE` instruction for MAX 10 devices to compensate for engineering delay.
- Modified PFL II to support version 5 of the Programmer Object File (POF) format. With POF format version 5, PFL II can send exact data to the device.
- Fixed a case where an internal error occured under certain conditions during SVF generation.
- Improved programming file generation error message handling.

1.2.2.6 Fitter

- Fixed a class of problems that can occur when Synopsys Design Contstraints (SDC) exceptions expand to a larger set of cells later in fitter. This condition caused an internal error when the system detected that physical synthesis attempted to delete cells with a timing exception.
- For Arria 10 devices, fixed a misleading critical warning where Shared HPS I/O pins were subject to the same check that ensures that the voltage on the HPS-dedicated I/O pins voltage corresponds to the declared VCCIO_HPS setting. The Shared HPS I/O voltage is independent of the VCCIO_HPS setting, and should not be subject to the check. This fix removes the misleading critical warning for the Shared HPS I/O pins.
- Fixed a problem that might occur when two logical DSP blocks are merged to share a single physical DSP location. This problem occured only if all of the following conditions were true:
  - The logical DSP blocks used independent 18x18 (`mode = "M18X18_FULL"`) precision mode where two logical instances can share a single physical block:
  - The logical DSPs were merged into a single physical location. The DSP merge appeared in the Netlist Optimizations report, and the DSP details report showed connected inputs for both the `ay` and `by` input signals.
  - The merge DSP block used the internal coefficient table of the DSP. That is, the **Uses Coefficient** column in the DSP details report shows `yes`, and the the `coefsela` and `coefselb` inputs are connected instead of the `ax` and `bx` inputs.
  - The coefficients stored in the internal table were to be interpreted as signed values.

  Under these circumstances, the multiplication assigned the B half of the physical DSP block incorrectly treated the coefficients as unsigned values, leading to an incorrect result for mulitplication operations involving a negative coefficient value.
- Improved hold timing closure during partial reconfiguration, when a clock is shared between a preserved static design partition and a partial reconfiguration design partition.

1.2.3 IP and IP Cores

Attention: Unless stated otherwise, the following IP issues apply to both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

40-100GbE IP Core

- Fixed an issue where the runtime statistics counter might read as "x" in simulation.
- Updated the PLL settings for increased reliability in Low-Latency 40G KR4 and 100G CAUI-4 IP Cores.
- Improved the reset and clock domain crossing robustness.

Arria 10 External Memory Interface (EMIF) IP Core

- Fixed the power-up OCT case such that the OCT block can properly be merged with other non-EMIF OCT blocks. The Arria 10 EMIF IP core can use power-up OCT (by default) or it can use user-mode OCT (if periodic OCT calibration is enabled).
- Quartus Prime software now shows correct I/O timing margins based on the data termination value that you select.
- Fixed a calibration bug that caused some groups in RLDRAM3 x36 width expanded mode to fail calibration on hardware.

Arria 10 Transceiver ATX PLL IP Core

- Added support for more than two profiles for the multi-profile dynamic reconfiguration feature.

Avalon Streaming (Avalon-ST) Dual-Clock FIFO IP Core

- Fixed the VHDL port width mismatch synthesis error seen in Quartus Prime Pro Edition software when the Avalon Streaming (Avalon-ST) Dual Clock FIFO IP code is not set to use packets and the SYMBOLS_PER_BEAT parameter is set to a value greater than 1.

DisplayPort IP Core

- For Arria 10 devices, updated the Design Example Transceiver reconfiguration update with the latest calibration register.

General Purpose I/O (GPIO) IP Core

- For Arria 10 devices, when you launch Qsys system integration tool, you are now warned that you the maximum interface frequency that you should use is 300 MHz.

I/O Phase-Locked Loop (IOPLL) IP Core

- For Arria 10 devices, fixed a potential issue where the fitter is unable to place an IOPLL or other periphery components that use or feed the IOPLL. This issue is associated with Fitter error messages such as the following error messages:

```
The Fitter cannot place 1 auto-promoted clock driver, which is within Altera
IOPLL <name of PLL>
```

```
Could not find path between source IOPLL and the auto-promoted clock driver
```

- Made the following changes:
  - Updated required PCIe settings previously specified in errata to correct values.
  - Enhanced fPLL settings to support alternative clocking for 50GE.
  - Changed calibration code to update minimum VCO gear settings for fPLL and CDR, and improve rx adaptation in PCIe Gen3.

PHYLite for Parallel Interfaces IP Core

- For Arria 10 devices, because of significant IR drop on the IO supply during calibration, the 300 Ohm and 400 Ohm input termination values are removed from the following I/O standards: SSTL-125, SSTL-135, and SSTL-15. Also, when you select a Class I or Class II I/O standard with an interface frequency greater than 533 MHz, you will get a warning. The selectable range of the **OCT enable size** has been changed from 0 - 7 to 0 - 4.

RapidIO IP Core

- Fixed an issue where the `ackID_status` value dies not increase even after it has received a packet-accepted control symbol from the link partner.

SerialLite III Streaming IP Core

- Fixed an unintended error condition where hardened PCS Tx FIFO overflow or underflow.

Video and Image Processing Suite

- Made timing improvements to meet 300MHz timing on Arria 10 devices with an –E2 or –I2 speed grade.

  Moved `Interrupt` register addresses due to component limitiations. The `Control` register for Clocked Video Output II (CVO II) has been modified as follows:

  Bits 8 and 9 of the `Control` register are the interrupt enables:

  — Setting bit 8 to 1 enables the status update interrupt.

  — Setting bit 9 to 1 enables the locked interrupt.

  The `Interrupt` register for CVO II has been modified as follows:

  Bits 8 and 9 of the `Interrupt` register are the interrupt status bits:

  — When bit 8 is asserted, the status update interrupt has triggered.

  — When bit 9 is asserted, the locked interrupt has triggered.

  — The interrupts stay asserted until a 1 is written to these bits.
- Fixed an issue where the Deinterlacer II IP core failed to output a correct control packet before video packets when using the Motion Adaptive High Quality (Sobel edge interpolation) deinterlacing algorithm without the video over film feature with cadence detection. This issue might have resulted in a blank screen.

1.2.4 JNEye

Attention: Unless stated otherwise, the following JNEye issues are associated with both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

- Made the following updates:

  — Configuration saving bug fix: Prevented random test pattern reset after channel model changes.

1.2.5 Intel FPGA SDK for OpenCL

Attention: Unless stated otherwise, the following Intel FPGA SDK for OpenCL issues are associated with both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

- Fixed a problem that caused windows emulation to fail when using generic math functions.
- Fixed an error where the compiler crashes with the following error message:

```
Error: Assert failure at StagingRegisterInsertion.cpp(354)
```

- Fixed an issue in the compiler where, in some cases, a single-precision floating-point accumulator would not synthesize properly, resulting in compilation error.
- Fixed an issue where the following assertions occurred for some designs during the `clang` stage of compilation:

```
Assertion `SLocOffset >= CurrentLoadedOffset && "Bad function choice"' failed.
```

- Added support for using `struct` data types as the inputs and output of OpenCL library functions.
- Fixed the following error that occured when casting some vector float constanct values:

```
Compiler Error: Unsupported constant expression detected. Aborting action.
```

- The OpenCL Library file specification (for both source and C model) now supports parent directory ("`..`") in relative file paths.
- Fixed a bug where the `ivdep` pragma and other pragmas were not applied to infinite loops.
- Implemented area savings for small channels if the return value for `write_channel_nb_altera` is ignored.
- Fixed an issue with the 2 sum mode 18x18 precision mode in variable-precision DSP blocks where the register stage has mixed secondary signals.
- Improved the RAM resource estimates for built-in OpenCL IP that are used in many OpenCL designs.
- Fixed a race condition in the kernel IRQ handler for OpenCL.
- For the Arria 10 GX FPGA Development Kit Reference Platform, updated the `base.qdb` file to be compatible with Quartus Prime Version 16.1.2.

1.2.6 Intel SoC FPGA Embedded Design Suite

- Completed the following updates:
  - Updated the `quartus_hps` command to detect the NAND flash bad block correctly.
  - Fixed inconsistent JTAG data transactions on Microsoft Windows 10 operating systems.
  - Added support for Micron M25P16 SPI flash devices.

1.3 Software Issues Resolved

Table 1. Customer Service Requests Resolved in the Quartus Prime Design Suite Version 16.1 Update 1

Customer Service Request Numbers Resolved					
365417	336787	369226	11066381	11085731	11257692
11260545	11263569	11264100	11267981	11271111	11274161

Table 2. Customer Service Requests Resolved in the Quartus Prime Design Suite Version 16.1 Update 2

Customer Service Request Numbers Resolved					
11227765	11238731	11252589	11255705	11256763	11259431
11262329	11263615	11264336	11265617	11268579	11271164
11272510	11273423	11274474	11275534	11277099	11279512
11280429	11285652	11282022			

1.4 Software Patches Included in Update Releases

Table 3. Software Patches included in the Quartus Prime Design Suite Version 16.1 Update 1

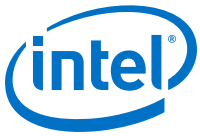
Software Version	Patch	Customer Service Request Number
Intel FPGA SDK for OpenCL	0.01cl	-
Quartus Prime Software 16.1	0.04	-

Table 4. Software Patches included in the Quartus Prime Design Suite Version 16.1 Update 2

Software Version	Patch	Customer Service Request Number
Quartus Prime Software 16.1	0.09	11227765
Quartus Prime Software 16.0.2	2.26	-
Quartus Prime Software 16.0.2	2.25	-
Quartus Prime Software 16.0.1	1.21	11252589
Quartus Prime Software 16.0	0.20	11275931
Quartus II 15.0	0.38	11271164
Quartus II 14.1.1	1.23	11279211
Quartus II 14.1	0.43	11277770
Quartus II 14.0	0.48	11277770

1.5 Known Issues and Workarounds

For information about known software issues, please visit the Intel FPGA Knowledge Base.



Related Links

- Intel FPGA Knowledge Database
- Intel FPGA Documentation: Release Notes
- Quartus Prime and Quartus II Software Support

1.6 Document Revision History

Date	Document Version	Changes
January 2017	2017.01.27	• Added Quartus Prime Design Suite version 16.1 update 2 information.
December 2016	2016.12.09	• Initial release with Quartus Prime Design Suite version 16.1 update 1 information.