Quartus Prime Design Suite Version 16.0 Update Release Notes

2016.08.01

RN-01080-16.0.2.0 Subscribe Send Feedback

This version of the *Quartus® Prime Design Suite Update Release Notes* describes the Quartus Prime Design Suite version 16.0 software update 2.

Quartus Prime Design Suite updates are cumulative; Update 2 includes Update 1.

The Quartus Prime Design Suite software update requires the Altera® Quartus Prime Standard Edition software release version 16.0 or the Altera Quartus Prime Pro Edition software release version 16.0. If you do not have either edition of the Quartus Prime software release version 16.0, please install it prior to installing any Quartus Prime Design Suite version 16.0 software updates to ensure the Quartus Prime software runs properly.

You may apply this software update to the Quartus Prime Lite Edition software, which supports the Arria® II, Cyclone® IV, Cyclone V, MAX® II, MAX V, and MAX 10 FPGA device families. The Quartus Prime Standard Edition software issues that apply to these device families also apply to the Quartus Prime Lite Edition software.

Related Information

- **Quartus Prime Standard Edition Software and Device Support Release Notes Version 16.0**
- **Quartus Prime Pro Edition Software and Device Support Release Notes Version 16.0**

Issues Addressed in Update 2

Attention: The 16.0.1 known issue involving PCI Express® (PCIe®) interfaces in Arria 10 devices, where Arria 10 PCIe settings might not be optimal for certain channel profiles and result in link Recoveries and Correctable errors, is now fixed. Altera recommends that you upgrade to the Quartus Prime software version 16.0.2.

Quartus Prime Standard Edition Software

Quartus Prime Software GUI

- Fixes an internal error in the RTL Viewer that might occur when loading a project that has an optimized buffer.

Quartus Prime Device Support

- Updates the timing model of the ASMI block to eliminate excessive output delay. This update affects Arria 10 devices.

  Note: This update changes the previously finalized timing model of Arria 10 10AX057, 10AS057, 10AX066, 10AS066, and 10AX115 devices.
- Sets final timing model attribute for Arria 10 10AX048 and 10AS048 devices.
- Updates the IBIS Writer for MAX 10 and Arria 10 device families to not print the IBIS comment character ("|") in pin names and to exclude transceiver pins from the Differential Pin section of the IBIS file.
- Finalizes the IBIS models for Arria 10 devices.
- Improves Arria 10 IBIS model correlation for I/Os using calibration.

Quartus Prime Compilation and Design Flows

- Fixes an internal error that might occur during compilation of an Arria 10 design if unused HSSI channels are preserved or if a fractional phase-locked loop (fPLL) instance does not have any clock outputs connected.

Fitter

- Fixes an internal error that might occur when `SPECTRAQ_PHYSICAL_SYNTHESIS` is enabled.
- For single-port memory blocks, fixes an issue that might occur under certain conditions when you set the memory block type to **Auto** with defined Read-During-Write (RDW) mode (New or Old Data). The single-port memory blocks might be mapped incorrectly to MLAB locations; this incorrect mapping does not guarantee the desired RDW behavior. With this fix, the single-port memory blocks now map to the dedicated memory blocks (that is, M9K, M10K, or M20K, depending on the family).
- Fixes a memory leak issue that might cause an out-of-memory error in the Fitter when compiling an Arria 10 design.
- Fixes a segmentation fault that occurs when you enable the **High Performance Effort** or the **Spectra-Q Physical Synthesis** option in Arria 10 designs that contain partitions.

Quartus Prime Programmer

- Fixes an internal error that occurs during the generation of programming files for Stratix® V, Arria V, and Cyclone V devices when both the Configuration via PCI Express (CvP) encryption and Partial Reconfiguration (PR) encryption features are enabled.
- Adds `quartus_cpf` command-line support to generate encrypted PR bitstreams for Stratix V, Arria V, and Cyclone V devices.
- For Arria 10 designs, fixes an error that prevents you from using the `quartus_cpf` command line to generate different key-type-encrypted bitstreams (for example, volatile or nonvolatile) using the Conversion Setup File (**.cof**).
- For Arria 10 devices, fixes an issue with the autodetect function that might cause the Programmer to report incorrect device identification.

TimeQuest Timing Analyzer

- Fixes an incorrect clock phase shift in the TimeQuest timing analysis for MAX 10 devices.

Quartus Prime Pro Edition Software

Quartus Prime Software GUI

- Fixes an issue where the Fitter fails without any error message if you run the Fitter in the Quartus Prime software GUI without a valid Quartus Prime Pro Edition software license. With this fix, the Fitter now displays an error message if the license is missing.
- Fixes an internal error that occurs in the Node Finder when you select **SignalTap II: post-fitting** under **Filter** and specify a **Look in** hierarchy path below a child partition.
- Fixes an issue where the Text Editor might encounter a fatal error unexpectedly when you activate it during a compilation or immediately after a compilation finishes.
- Fixes an internal error in the RTL Viewer that might occur when loading a project that has an optimized buffer.

Quartus Prime Device Support

- Updates the timing model of the ASMI block to eliminate excessive output delay. This update affects Arria 10 devices.

  Note: This update changes the previously finalized timing model of Arria 10 10AX057, 10AS057, 10AX066, 10AS066, and 10AX115 devices.
- Sets final timing model attribute for Arria 10 10AX048 and 10AS048 devices.
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- Finalizes the IBIS models for Arria 10 devices.
- Improves Arria 10 IBIS model correlation for I/Os using calibration.

Quartus Prime Compilation and Design Flows

- Fixes an internal error that might occur during compilation of an Arria 10 design if unused HSSI channels are preserved or if a fractional phase-locked loop (fPLL) instance does not have any clock outputs connected.

Fitter

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- Fixes a memory leak issue that might cause an out-of-memory error in the Fitter when compiling an Arria 10 design.
- Fixes a segmentation fault that occurs when you enable the **High Performance Effort** or the **Spectra-Q Physical Synthesis** option in Arria 10 designs that contain partitions.

Quartus Prime Programmer

- For Arria 10 designs, fixes an error that prevents you from using the `quartus_cpf` command line to generate different key-type-encrypted bitstreams (for example, volatile or nonvolatile) using the Conversion Setup File (**.cof**).
- For Arria 10 devices, fixes an issue with the autodetect function that might cause the Programmer to report incorrect device identification.

IP and IP Cores

Attention: Unless stated otherwise, the following IP issues apply to both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

10GBASER PHY IP Core

- Fixes an issue that causes an inaccurate result during rate match.

Altera PLL IP Core

- Fixes an issue that causes an incorrect frequency difference calculation when using advanced transmit (ATX) PLL with Arria 10 devices. In some cases, the incorrect frequency difference calculation might cause an invalid ciritcal warning message to appear.

EMIF IP

- Fixes an issue where LPDDR2 calibration can only detect a small read window when MAX 10 boot from Flash is enabled. This fix is necessary to improve the robustness of the LPDDR2 EMIF calibration algorithm for MAX 10 devices. This issue affects the Quartus Prime Standard Edition software.

HSSI IP Core

- Fixes an Arria 10 fPLL simulation issue that might cause the incorrect alignment of the output clock phase.

JESD204B IP Core

- Fixes an issue where the SignalTap™ II generation file is missing in the Nios® II processor control unit design example. Prior to this fix, the Quartus Prime software could not generate the SignalTap II file in the Nios II processor control unit design example because of a missing XML input file.

Low Latency Ethernet 10G MAC IP Core

- Fixes an issue that causes an inaccuracy in the IEEE1588 operation of the IP when the **IEEE1588** option is enabled.

Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Cores

- Improves reset robustness for the low-latency 40GBASE-KR4 Ethernet PHY IP core.

PCI Express Hard IP Core

Attention: The 16.0.1 known issue involving PCI Express (PCIe) interfaces in Arria 10 devices, where Arria 10 PCIe settings might not be optimal for certain channel profiles and result in link Recoveries and Correctable errors, is now fixed. Altera recommends that you upgrade to the Quartus Prime software version 16.0.2.

- Fixes clock data recovery (CDR) PLL and physical medium attachment (PMA) issues in Arria 10 PCIe IP. Altera strongly recommends that you upgrade to the current Quartus Prime Design Suite Update version.

  Note: This fix affects previously finalized bit settings for Arria 10 devices.
- Fixes an issue where the `tx_cred_fc_hip_const` interface is not functional in the Single Root I/O Virtualization (SR-IOV) implementation.
- Updates the transceiver configuration settings in the Arria 10 PCIe dynamic design examples.
- Updates the HSSI calibration code to fix an issue that affects the PCIe interfaces in Arria 10 devices.

  Note: This update affects previously finalized bit settings for Arria 10 10AX057, 10AS057, 10AX066, 10AS066, and 10AX115 devices.
- Includes the following SR-IOV2 core changes:
  - Fixes the Block Design File (BDF) capture feature for 2K functions.
  - Turns on Function Level Reset by default for SR-IOV functionality.

  Note: The SR-IOV2 core has a preliminary status in this current release.

SerialLite III Streaming IP Core

- Addresses the following changes:
  - Removes the unused input port `xcvr_pll_ref_clk` in Arria 10 SerialLite III Streaming Source-only designs because the unused port causes an error message to appear.
  - Removes duplicated Synopsys Design Constraints (SDC) constraints from the **seriallite_iii_streaming_demo.sdc** file. The Quartus Prime software only refers to the constraints listed in the Arria 10 SerialLite III Streaming IP's **.sdc** file.

Serial Digital Interface II IP Core

- Fixes a lock-up issue that occurs when you instantiate multiple triple-rate-mode or multirate-mode RX instances that request for reconfiguration. This issue affects Arria 10 designs.

Triple Speed Ethernet IP Core

- Fixes an issue where some TSE variants are missing the SDC constraints for clock crossers, which cause timing violations. This issue affects the TSE variants that meet all of the following criteria:

  1. Core variation —10/100/1000Mb Ethernet MAC
  2. Does not include statistics counters
  3. One of the following options is enabled:
     - MAC 10/100 half duplex support
     - ECC protection
     - Timestamping
- Fixes an issue that causes the synchronizer that synchronizes `xon_gen` and `xoff_gen` to reset incorrectly.

DSP Builder Advanced Blockset

- Fixes the broken links to HTML Help pages from the index of the DSP Builder Advanced Example designs.

Altera SDK for OpenCL

Attention: Unless stated otherwise, the following Altera SDK for OpenCL™ issues are associated with both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

- Fixes an issue that might cause functional failures when using the Altera SDK for OpenCL to program Arria 10 devices.

Issues Addressed in Update 1

Attention: A known issue involving PCI Express (PCIe) interfaces in Arria 10 devices exists in the Quartus Prime software version 16.0 update 1. Arria 10 PCIe settings might not be optimal for certain channel profiles, resulting in link Recoveries and Correctable errors. For more information, refer to the **Known Issues and Workarounds** section.

Quartus Prime Standard Edition Software

Quartus Prime Device Support

- Changes the previously finalized timing model and configuration settings for Arria 10 10AX115 devices.
- Updates the timing model for some routing wires in Arria 10 devices except the 10AX115 devices.
- Sets final timing model attribute for Arria 10 10AX057, 10AS057, 10AX066, and 10AS066 devices.
- Updates the power model for Arria 10 10AX057, 10AS057, 10AX066, and 10AS066 devices.
- Sets final power model attribute for Arria 10 10AX057, 10AS057, 10AX066, and 10AS066 devices.
- Enables the version-compatible database feature for Arria 10 devices.

Quartus Prime Software Installation

- Changes the software installation process on Windows because the software update is available as a TAR file instead of an EXE file:

  1. Download the TAR file.
  2. Extract the files into a temporary directory.
  3. One of the extracted files is the **QuartusSetup-<*version*>-windows.exe** file. Run this **.exe** file from the temporary directory.

Quartus Prime Compilation and Design Flows

- Fixes an error in the Design Space Explorer II where the Linux secure shell (SSH) loads the **libcrypto.so** library from the **quartus/linux64** directory instead of the operating system.
- Fixes an error in timing analysis that might cause an error when using explicit atypical timing corners. This error affects designs that target Arria 10 devices.
- Fixes an error that prevents the `qexit -<return_code>` command from setting the correct return code of a Quartus Prime Tcl script.
- Updates the metastability reports to no longer show synchronizer chains that start with nonexistent compiler-generated registers.
- Fixes an error in synthesis involving ROM inference, that is, the implementation of RTL logic using an initialized memory block. Prior to this fix, the initial power-up state of the ROM output register might cause incorrect logic.
- Fixes a fatal error in synthesis that is related to state machine processing.

Quartus Prime Programmer

- Increases the JTAG configuration delay time for MAX 10 devices.
- Disables an illegal encryption key programming (EKP) verification operation in the Programmer for MAX 10 devices.

Fitter

- For core registers that are packed into the periphery to increase I/O performance, enhances the Fitter to optimize the transfer of these core registers into the core. This enhancement also provides higher timing slack. Prior to this enhancement, the Fitter did not properly optimize the transfer of these registers into the core.
- Fixes an issue where assigning a reserved pin in your design causes the PowerPlay Power Analyzer to encounter a fatal error.
- Fixes an issue with the HSSI TX BTI mitigation soft IP. Prior to this fix, if you used the QSF assignment `PRESERVE_UNUSED_XCVR_CHANNEL`, you must recompile your design. This issue affects all Arria 10 devices.

Simulation

- Fixes the Arria 10 PLL simulation model to address the failure to lock in corner-case reconfiguration.

Quartus Prime Pro Edition Software

Quartus Prime Device Support

- Changes the previously finalized timing model and configuration settings for Arria 10 10AX115 devices.
- Updates the timing model for some routing wires in Arria 10 devices except the 10AX115 devices.
- Sets final timing model attribute for Arria 10 10AX057, 10AS057, 10AX066, and 10AS066 devices.
- Updates the power model for Arria 10 10AX057, 10AS057, 10AX066, and 10AS066 devices.
- Sets final power model attribute for Arria 10 10AX057, 10AS057, 10AX066, and 10AS066 devices.
- Enables the version-compatible database feature for Arria 10 devices.

Quartus Prime Software Installation

- Changes the software installation process on Windows because the software update is available as a TAR file instead of an EXE file:

  1. Download the TAR file.
  2. Extract the files into a temporary directory.
  3. One of the extracted files is the **QuartusSetup-<*version*>-windows.exe** file. Run this **.exe** file from the temporary directory.

Quartus Prime Compilation and Design Flows

- Fixes an error in the Design Space Explorer II where the Linux secure shell (SSH) loads the **libcrypto.so** library from the **quartus/linux64** directory instead of the operating system.
- Fixes an error that prevents the `qexit -<return_code>` command from setting the correct return code of a Quartus Prime Tcl script.
- Fixes an issue where the messages section is missing from the synthesis report generated in the Windows version of the Quartus Prime Pro Edition software. This issue occurs when you perform synthesis in the command line mode.
- Fixes an issue with the **Suppress Messages with Matching ID** feature where the text comparison is incorrect. This fix also ensures that the Quartus Prime Pro Edition software imports the suppressed messages file while opening a project.
- Fixes an issue where the name of a Qsys IP file (**.qsys**) that starts with the string "error" might cause the IP generation step of the Quartus Prime Pro Edition software design flow to fail, even if the design has no errors.
- Fixes an error in timing analysis that might cause an error when using explicit atypical timing corners. This error affects designs that target Arria 10 devices.
- Updates the metastability reports to no longer show synchronizer chains that start with nonexistent compiler-generated registers.
- Fixes an error in synthesis involving ROM inference, that is, the implementation of RTL logic using an initialized memory block. Prior to this fix, the initial power-up state of the ROM output register might cause incorrect logic.
- Fixes an internal error in synthesis that might occur when a module interface uses an array of structures.
- Fixes an internal error that might occur when compiling an Arria 10 design that uses the Altera Debug Master Endpoint (ADME) IP within a partition.
- Cuts false paths in the Synopsys Design Constraints (SDC) for the Interlaken design example.

Fitter

- For core registers that are packed into the periphery to increase I/O performance, enhances the Fitter to optimize the transfer of these core registers into the core. This enhancement also provides higher timing slack. Prior to this enhancement, the Fitter did not properly optimize the transfer of these registers into the core.
- Fixes an issue where assigning a reserved pin in your design causes the PowerPlay Power Analyzer to encounter a fatal error.
- Fixes an issue that might cause incorrect results when you perform partial reconfiguration (PR) on an Arria 10 design that has a PR partition with unconnected boundary parts.
- Fixes an issue with the HSSI TX BTI mitigation soft IP. Prior to this fix, if you used the QSF assignment `PRESERVE_UNUSED_XCVR_CHANNEL`, you must recompile your design. This issue affects all Arria 10 devices.

Simulation

- Fixes the Arria 10 PLL simulation model to address the failure to lock in corner-case reconfiguration.

IP and IP Cores

Attention: Unless stated otherwise, the following IP issues apply to both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

1G/2.5G/5G/10G Multi-rate Ethernet PHY IP Core

- Updates the parameter editor GUI for the 25G Ethernet PHY IP core to make the **Link Fault** check box visible.

25G/50G Ethernet IP Core

- For Arria 10 IP, removes the **Enable ODI** feature from the IP parameter editor GUI.
- For 25G Ethernet Reed-Solomon Forward Error Correction (RSFEC) IP core, fixes an issue where the RX status vector might incorrectly indicate the packet type when RSFEC is enabled.
- Removes the **TX CRC passthrough** option in the 50G Ethernet IP parameter editor GUI.

Altera GPIO IP Core

- Turns on Low Voltage IO Buffer mode for the following I/O standards:
  - sstl12 c1
  - sstl12 c2
  - sstl125 c1
  - sstl125 c2
  - sstl135 c1
  - sstl135 c2
  - differential sstl 12 C1
  - differential sstl 12 C2
  - differential sstl 125 C1
  - differential sstl 125 C2
  - differential sstl 135 C1
  - differential sstl 135 C2

Altera IOPLL IP Core

- Fixes a Qsys generation issue that affects designs that target Cyclone IV or Stratix IV devices and use ALTPLL IP in Qsys.

Arria 10 fPLL IP Core

- Updates the IP and block setting rules to support Optical Transport Network (OTN) direct mode.

DisplayPort IP Core

- Fixes an issue where the `DPRX_RX_STATUS` register value is incorrect when `MAX_LANES_COUNT` has a value of 1 or 2.

EMIF IP

- For Arria 10 EMIF IP, fixes some DDR4 LRDIMM hardware issues that might cause DDR4 LRDIMM calibration to fail in hardware.
- For Arria 10 EMIF IP, updates the IP parameter editor GUI for DDR4 RDIMM and LRDIMM. With this update, the GUI now accepts individual RDIMM or LRDIMM serial presence-detect (SPD) data directly without any manual encoding. The IP then calculates the encoded RCD and DB configuration settings.

  If you upgrade from a previous version of the IP that uses the encoded values, the new version of the IP will accept these encoded values.
- Removes the following invalid Arria 10 EMIF IP parameter editor GUI options from the **Diagnostics** tab:
  - Calibration Address 0
  - Calibration Address 1
  - Enable automatic calibration after reset

  These options are only valid for nondestructive calibration, which is not a publicly-visible feature. Contact Intel's Programmable Solutions Group if you require access to nondestructive calibration.
- Addresses the following changes:
  - Fixes an Arria 10 EMIF IP simulation-specific error to allow 17-bit address width to be properly recognized when you enable Abstract PHY.
  - Fixes an error in the memory model to support SODIMM.

HPS IP Core

- Fixes an issue in the HPS IP component for Arria 10 SoCs. With this fix, the SoC Embedded Design Suite (SoC EDS) can now access the proper HPS DMA command to address some cache coherency issues in the HPS preloader.
- For Arria 10 HPS I2C pins, fixes an issue where the Quartus Prime software does not set the I2C I/O open drain bits properly.
- Fixes a typo in an HPS IP component error message that appears in Qsys.
- Fixes a typo in a general I/O pin placement error message that causes confusion when you use the Arria 10 HPS EMIF. Prior to this fix, in some situations where you could only use the input pins that were in the same I/O bank as Arria 10 HPS EMIF, the error message falsely indicated that you could only place output pins.

JESD204B IP Core

- Revises the IP core test bench bonding configurations and ATX PLL parameter settings.

Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Cores

- Fixes an fPLL compilation error in the 4-lane 100 Gigabit Attachment Unit Interface (CAUI-4) Forward Error Correction (FEC) variant of the low latency 100Gbps Ethernet IP core. This error affects Arria 10 devices.
- For the 40GBASE-KR4 IP core, fixes an error to ensure that timing closure results for the Auto Negotiation module are accurate irrespective of the Auto Negotiation master channel.
- Adds URLs of the design example user guides to the IP parameter editor GUI.

Partial Reconfiguration IP Core

- Addresses the following issues:
  - Fixes a metastability issue that might occur in the Arria 10 `prblock` primitive.
  - Fixes a glitch issue that might occur when multiplexing the IP's system clock and JTAG clock.

PCI Express Hard IP Core

Attention: A known issue involving PCI Express (PCIe) interfaces in Arria 10 devices exists in the Quartus Prime software version 16.0 update 1. Arria 10 PCIe settings might not be optimal for certain channel profiles, resulting in link Recoveries and Correctable errors. For more information, refer to the **Known Issues and Workarounds** section.

- For Arria 10 designs using the PCIe hard IP, adds timing arcs from the PCIe hard IP outputs `tl_cfg_add` and `tl_cfg_ctl`. This addition is necessary because of a change to the finalized Arria 10 timing models.
- Fixes an issue where a timing arc is missing from the `tl_cfg_add/tl_cfg_ctl` bus.
- Updates the Example Design Generation callback to fix an issue regarding the inability to generate Dynamic Example Design in Windows for Arria 10 devices.
- Addresses the following changes:
  - Enables the PCIe Link Training Status State Machine (LTSSM) state to hold in recovery for a fixed time on subsequent reentry to Gen3 or Gen1/Gen2 speeds.
  - Sets the default far-end preset TX to P8.
- Address the following issues:
  - Sets the 256-bit Root Port to PRELIMINARY only with the Avalon®-MM interface and not the Avalon-ST interface. The 256-bit Avalon-MM mode will appear as PRELIMINARY.
  - SR-IOV supports target-only simulation and does not require an additional **Simulation Option** tab in the GUI because there is only one application endpoint.

RapidIO I IP Core

- Fixes the Source Operations (0x18) and Destination Operations (0x1C) capability registers to reflect the actual settings in the RapidIO IP parameter editor.

SerialLite III Streaming IP Core

- Fixes incorrect error checking and correction (ECC) error bits in `tx_error`.
- Addresses the following changes:
  - Adds user input support for lane rate.
  - Removes transceiver on-die instrumentation (ODI) options from the IP parameter editor GUI.
  - Updates the parameter description in the IP parameter editor GUI.

DSP Builder Advanced Blockset

- Fixes an issue that affects DSPBA-generated VHDL. Prior to this fix, when your VHDL design had a mixed-sign multiplication, `UNSIGNED` constants that were stored in the DSP block ROM were stored as `SIGNED`, resulting in incorrect multiplication results.

  This issue does not affect DSPBA-generated Verilog.

Altera SDK for OpenCL

Attention: Unless stated otherwise, the following Altera SDK for OpenCL issues are associated with both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

- Increases the number of upper bits within the global memory pointer that the AOCL uses to accommodate device IDs. This adjustment increases the allocated bit width to 5 bits so that the runtime can account for a maximum of 32 devices.
- Fixes a fatal error that might occur in the Altera Offline Compiler when it compiles a work-item-invariant computation that has a high fan-out.

Software Issues Resolved

Table 1: Software Issues Resolved in the Quartus Prime Design Suite Version 16.0 Update 2

Description	Quartus Prime Edition Affected	Workaround
The LTSSM for the Arria 10 PCIe link might enter into the Recovery state after initial link training. The problem occurs because the transceiver settings for the Arria 10 PCIe IP core are not optimal in the Quartus Prime software versions 16.0 and 16.0.1. The existing settings might cause bit errors, resulting in link Recoveries and Correctable errors for certain channel loss profiles. These errors are only observed in hardware, and not in simulation or during design compilation.	Standard and Pro	This issue is fixed in the Quartus Prime software version 16.0.2. Altera recommends that you upgrade to this software version.

Table 2: Customer Service Requests Resolved in the Quartus Prime Design Suite Version 16.0 Update 2

Customer Service Request Numbers Resolved					
11213587	11213799	11222180	11225366	11228086	11228210
11230501	11232973	11233411	11233921	11234730	11236148
11236399	11237723	11239339	11240453	11243135	—

Table 3: Customer Service Requests Resolved in the Quartus Prime Design Suite Version 16.0 Update 1

Customer Service Request Numbers Resolved					
11168817	11206718	11213610	11219862	11219477	11220036

Software Patches Included in Update Releases

Table 4: Software Patches Included in the Quartus Prime Design Suite Version 16.0 Update 2

Software Version	Patch	Customer Service Request Number
Quartus Prime Software 16.0.1	1.01	11213799
Quartus Prime Software 16.0.1	1.05	—
Quartus Prime Software 16.0.1	1.09	11225366
Quartus Prime Software 16.0.1	1.10	11232973
Quartus Prime Software 16.0.1	1.11	11228210
Quartus Prime Software 16.0	0.05	11228210
Quartus Prime Software 15.1.2	2.23	11213799

Table 5: Software Patches included in the Quartus Prime Design Suite Version 16.0 Update 1

Software Version	Patch	Customer Service Request Number
Altera SDK for OpenCL 16.0	0.01cl	11220036
Quartus Prime Software 15.1.2	2.29	11219477

Known Issues and Workarounds

This section provides information about the following known issues that affect the Altera SDK for OpenCL software version 16.0 update 2.

Description	Workaround
If you program an Arria 10 device by targeting the 16.0.2 version of the Arria 10 GX FPGA Development Kit Reference Platform and you carry out a long sequence (>500 times) of programming via Partial Reconfiguration while running the host program, you might encounter incorrect application behavior.	Allow the host program to terminate. If you determine that the application behaved incorrectly, reexecute the host program. For more information, refer to the **Altera Knowledge Database**.

This section provides information about the following known issues that affect the Quartus Prime software version 16.0 update 1.

Description	Quartus Prime Edition Affected	Workaround
If you use Google Chrome to load locally-installed Quartus Prime Help, you might be prompted to disable some JavaScript functionality.	Standard and Pro	For the best viewing experience using Google Chrome, navigate to **http://quartushelp.altera.com/current/index.htm** to access Quartus Prime Help. For more workaround options, refer to the **Altera Knowledge Database**.
The LTSSM for the Arria 10 PCIe link might enter into the Recovery state after initial link training. The problem occurs because the transceiver settings for the Arria 10 PCIe IP core are not optimal in the Quartus Prime software versions 16.0 and 16.0.1. The existing settings might cause bit errors, resulting in link Recoveries and Correctable errors for certain channel loss profiles. These errors are only observed in hardware, and not in simulation or during design compilation.	Standard and Pro	This problem will be addressed in the Quartus Prime software version 16.0.2. For more information, refer to the **Altera Knowledge Database**.

For information about known software issues, please visit the Altera Knowledge Database.

Related Information

- **Altera Knowledge Database**
- **Altera Documentation: Release Notes**
- **Quartus Prime and Quartus II Software Support**

Document Revision History

Table 6: Quartus Prime Design Suite Version 16.0 Updates Document Revision History

Date	Document Version	Changes
August 2016	2016.08.01	Added Quartus Prime Design Suite version 16.0 update 2 information.
June 2016	2016.06.10	Added Quartus Prime Design Suite version 16.0 update 1 information.