Quartus Prime Design Suite Version 15.1 Update Release Notes

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This version of the *Quartus® Prime Design Suite Update Release Notes* describes the Quartus Prime Design Suite version 15.1 software update 2.

Quartus Prime Design Suite updates are cumulative; Update 2 includes Update 1.

The Quartus Prime Design Suite software update requires the Altera® Quartus Prime Standard Edition software release version 15.1 or the Altera Quartus Prime Pro Edition software release version 15.1. If you do not have either edition of the Quartus Prime software release version 15.1, please install it prior to installing any Quartus Prime Design Suite version 15.1 software updates to ensure the Quartus Prime software runs properly.

You may apply this software update to the Quartus Prime Lite Edition software, which supports the Arria® II, Cyclone® IV, Cyclone V, MAX® II, MAX V, and MAX 10 FPGA device families. The Quartus Prime Standard Edition software issues that apply to these device families also apply to the Quartus Prime Lite Edition software.

Related Information

- **Quartus Prime Standard Edition Software and Device Support Release Notes Version 15.1**
- **Quartus Prime Pro Edition Software and Device Support Release Notes Version 15.1**

Issues Addressed in Update 2

Quartus Prime Standard Edition Software

Quartus Prime Software GUI

- Fixes an error that occurs when the Quartus Prime Initialization File (**.ini**) contains an invalid entry.

Quartus Prime Device Support

- Changes the adaptation start sequence in TTK to allow more control by the uC.
- Includes the following updates to MAX 10 timing models:
  - Finalizes the timing models for MAX 10 10M16, 10M25, 10M40, and 10M50 devices. With this update, all MAX 10 devices now have final timing models.
  - Updates the timing model for the Flash block in all MAX 10 devices to eliminate a false minimum pulse width violation on the `XE_YE` signal and a false hold violation on `DRDOUT` registers.
- Enables the programming files for Arria 10 10AX048 engineering sample (ES) and 10AS048 ES devices.
- Adds the MAX 10 10M04SAE144C8G, 10M04SAE144I7G, 10M04SAU169I7G, and 10M16SAE144I7G devices to the list of supported devices.
- Updates the router to avoid using a small set of routing wires that are no longer available for use. This update affects Arria 10 10AX115, 10AX048, and 10AS048 devices.

Quartus Prime Compilation and Design Flows

- Fixes an issue that affects the `coreclkout` clock divider settings in Arria 10 PCI Express® (PCIe®) hard IP.
- Reduces the initialization time of several Quartus Prime executables.
- Fixes an issue where a missing file causes a VHDL simulation error in designs that target Arria II GX devices on Windows platform.
- Fixes the ability of the Design Space Explorer II (DSE II) to process extra LSF assignments. With this fix, you can now enter the extra settings via one of the following methods:
  - In the **Additional remote settings** entry box under **Setup** in the DSE II GUI.
  - On the command line, include the `--lsf-farm-args _extra_args=<value>` argument, where <*value*> is an extra LSF setting.
  - In the ***<revision>*.dse** file, include the `lsf_farm_args=_extra_args=<value>` line, where <*value*> is an extra LSF setting.
- Fixes the Autosweep result table in the Transceiver Toolkit so that it lists the entries chronologically by default.

Qsys

- In Qsys, under **Pin Mux and Peripherals** for the Arria 10 HPS IP component, removes the PLL pull-down menu from the **IP Selection** tab.
- Enables you to expose the Arria 10 HPS Ethernet MAC (EMAC) IP's Precision Time Protocol (PTP) timestamp interface signals in Qsys. Prior to this enhancement, the signals were available to the FPGA core fabric when you connected the Arria 10 HPS EMAC IP to the HPS-dedicated pins, but the active HPS EMAC PTP ports were not exposed in Qsys.
- Fixes an issue in Qsys where the HPS IP component improperly configures the HPS MPU clock speed for the fastest Arria 10 SX device (speed grade 1). This issue does not affect other Arria 10 device speed grades.
- Addresses the following Qsys issues that relate to the Arria 10 HPS IP component:
  - In the Arria 10 HPS atom's **Pin Mux and Peripherals** GUI widget, fixes an issue where the **Advanced FPGA Placement** tab incorrectly overwrites the IP placed in the **Advanced HPS** tab.
  - Disables the FPGA options associated with the IP that are placed in the HPS.

Fitter

- Adds a placement legality check for PCIe Gen3 PIPE IP interfaces for Arria 10 speed grade 2 and speed grade 3 devices.

  This legality check is necessary because timing requirement is not met if you place the master channel at HSSI channels that link to hard IP for Arria 10 speed grade 2 and speed grade 3 devices. You must change the master channel to a different index to avoid hard IP channel locations, change the location of the master channel to avoid hard IP channel locations, or change the device speed grade to 1.
- Fixes an internal error that occurs when compiling an Arria 10 design that has illegal settings of pre-adder input clocks.
- For Arria 10 designs, fixes a segmentation fault that occurs when you enable the **Performance (High effort)** or **Spectra-Q Physical Synthesis** compiler setting.
- For Arria 10 designs, fixes an issue that causes incorrect I/O slew rate settings under certain conditions.

Quartus Prime Programmer

- Fixes an internal error in the Programmer that might occur when you program a MAX 10 device using a Programmer Object File (**.pof**) generated in earlier versions of the Quartus II software.
- Updates the factory Serial Flash Loader (SFL) image for Arria 10 10AS048 ES and 10AX048 ES devices.
- Updates the POF IDs and the Device JTAG IDs for Arria 10 devices.
- Fixes the computation span for the error detection cycle redundancy check (EDCRC) engine. This fix affects Arria 10 10AX048 and 10AS048 devices.
- Fixes an issue where MAX 10 POF programming using the Jam™ Standard Test and Programming Language (STAPL) Format File (**.jam**) and JAM Byte Code File (**.jbc**) fails when the JTAG chain contains one or more non-MAX 10 devices.

TimeQuest Timing Analyzer

- Removes the **Multicorner Datasheet Report** folder from the TimeQuest compilation report because the folder is blank.
- Fixes an issue that might cause long compilation times for designs containing the `set_net_delay` assignment.
- Fixes an issue that causes Arria 10 designs with many `set_max_skew` assignments to have very long compilation run times.

Quartus Prime Pro Edition Software

Quartus Prime Software GUI

- Fixes an error that occurs when the Quartus Prime Initialization File (**.ini**) contains an invalid entry.

Quartus Prime Device Support

- Changes the adaptation start sequence in TTK to allow more control by the uC.
- Fixes an issue that causes incorrect operation after performing Partial Reconfiguration on Arria 10 devices. This issue affects Arria 10 designs that use Partial Reconfiguration, including Altera SDK for OpenCL™ designs.
- Enables the programming files for Arria 10 10AX048 engineering sample (ES) and 10AS048 ES devices.
- Updates the router to avoid using a small set of routing wires that are no longer available for use. This update affects Arria 10 10AX115, 10AX048, and 10AS048 devices.

Quartus Prime Compilation and Design Flows

- Fixes an issue that affects the `coreclkout` clock divider settings in Arria 10 PCI Express (PCIe) hard IP.
- Reduces the initialization time of several Quartus Prime executables.
- Fixes a VHDL synthesis issue where statements in a VHDL process might be executed in the wrong order.
- Fixes an issue where performing Partial Reconfiguration on an Arria 10 design might cause incorrect design functionality.
- Fixes the ability of the Design Space Explorer II (DSE II) to process extra LSF assignments. With this fix, you can now enter the extra settings via one of the following methods:
  - In the **Additional remote settings** entry box under **Setup** in the DSE II GUI.
  - On the command line, include the `--lsf-farm-args _extra_args=<value>` argument, where <*value*> is an extra LSF setting.
  - In the ***<revision>*.dse** file, include the `lsf_farm_args=_extra_args=<value>` line, where <*value*> is an extra LSF setting.
- Fixes the Autosweep result table in the Transceiver Toolkit so that it lists the entries chronologically by default.

Qsys

- In Qsys, under **Pin Mux and Peripherals** for the Arria 10 HPS IP component, removes the PLL pull-down menu from the **IP Selection** tab.
- Enables you to expose the Arria 10 HPS Ethernet MAC (EMAC) IP's Precision Time Protocol (PTP) timestamp interface signals in Qsys. Prior to this enhancement, the signals were available to the FPGA core fabric when you connected the Arria 10 HPS EMAC IP to the HPS-dedicated pins, but the active HPS EMAC PTP ports were not exposed in Qsys.
- Fixes an issue in Qsys where the HPS IP component improperly configures the HPS MPU clock speed for the fastest Arria 10 SX device (speed grade 1). This issue does not affect other Arria 10 device speed grades.
- Addresses the following Qsys issues that relate to the Arria 10 HPS IP component:
  - In the Arria 10 HPS atom's **Pin Mux and Peripherals** GUI widget, fixes an issue where the **Advanced FPGA Placement** tab incorrectly overwrites the IP placed in the **Advanced HPS** tab.
  - Disables the FPGA options associated with the IP that are placed in the HPS.

Fitter

- Fixes an internal error that occurs in the Fitter when you compile an Arria 10 design that has LogicLock™ Plus constraints on logic array block (LAB) flipflops with the `SPECTRAQ_PHYSICAL_SYNTHESIS` compiler setting enabled. This internal error is especially likely to occur in Altera SDK for OpenCL compilation flows that use Partial Reconfiguration because they apply LogicLock Plus constraints internally.

  Note: The `SPECTRAQ_PHYSICAL_SYNTHESIS` setting is enabled automatically when you set `OPTIMIZATION_MODE` to `AGGRESSIVE PERFORMANCE`.
- Adds a placement legality check for PCIe Gen3 PIPE IP interfaces for Arria 10 speed grade 2 and speed grade 3 devices.

  This legality check is necessary because timing requirement is not met if you place the master channel at HSSI channels that link to hard IP for Arria 10 speed grade 2 and speed grade 3 devices. You must change the master channel to a different index to avoid hard IP channel locations, change the location of the master channel to avoid hard IP channel locations, or change the device speed grade to 1.
- Fixes an internal error that occurs when compiling an Arria 10 design that has illegal settings of pre-adder input clocks.
- For Arria 10 designs, fixes a segmentation fault that occurs when you enable the **Performance (High effort)** or **Spectra-Q Physical Synthesis** compiler setting.
- For Arria 10 designs, fixes an issue that causes incorrect I/O slew rate settings under certain conditions.

Quartus Prime Programmer

- Updates the factory Serial Flash Loader (SFL) image for Arria 10 10AS048 ES and 10AX048 ES devices.
- Updates the POF IDs and the Device JTAG IDs for Arria 10 devices.
- Fixes the computation span for the error detection cycle redundancy check (EDCRC) engine. This fix affects Arria 10 10AX048 and 10AS048 devices.
- Fixes an issue where MAX 10 POF programming using the Jam Standard Test and Programming Language (STAPL) Format File (**.jam**) and JAM Byte Code File (**.jbc**) fails when the JTAG chain contains one or more non-MAX 10 devices.

TimeQuest Timing Analyzer

- Removes the **Multicorner Datasheet Report** folder from the TimeQuest compilation report because the folder is blank.
- Fixes an issue that might cause long compilation times for designs containing the `set_net_delay` assignment.
- Fixes an issue that causes Arria 10 designs with many `set_max_skew` assignments to have very long compilation run times.

IP and IP Cores

Attention: Unless stated otherwise, the following IP issues apply to both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

Altera On-Chip Flash IP Core

- Disables an invalid timing warning message for the IP in designs targeting MAX 10 devices. The invalid timing warning message appears in the Quartus Prime Standard Edition software.

Altera Soft LVDS IP Core

- For MAX 10 Soft LVDS IP targeting a single supply device, includes a warning message that appears if the specified data rate exceeds the maximum data rate limit. This addition affects the Quartus Prime Standard Edition software.

Altera Temperature Sensor IP Core

- Includes a dummy simulation model in the IP core to prevent an error from occurring during simulator elaboration.

Arria 10 10GBASE-KR Ethernet PHY IP Core

- Updates KR IP variants to reflect latest Rules Based Configuration (RBC) settings.
- Updates the KR IP for improved reliability and better backplane performance.

Arria 10 fPLL IP Core

- Updates the IP to internally connect `cal_done` from the Avalon® Memory-Mapped (Avalon-MM) atom to the `rst_n` port of the fPLL atom. With this fix, the fPLL in non-PCIe hard IP designs is reset whenever power-up calibration or user-requested recalibration is performed. Prior to this update, the Quartus Prime software could not reset the fPLL in the following scenarios because the fPLL's `pll_powerdown` input was internally disconnected by default:
  - When dynamically reconfiguring the fPLL from integer mode to fractional mode, the output clock frequency might be incorrect if the PLL was not reset before calibration.
  - Without a reset, when the fPLL drove clocks to the FPGA fabric and used multiple output counters, there might be phase misalignment in the outputs.

  Note: This fix might cause fPLL instability issues in ES Revision C silicon. As a workaround, add the following global `QSF MACRO` setting in your design:

  ```
  set_global_assignment -name VERILOG_MACRO
  "ALTERA_XCVR_A10_DISABLE_RESET_CONNECTED_TO_CAL_BUSY=1"
  ```
- For Arria 10 fPLL IP, fixes an issue that causes the **Enable analog reset** option to be missing in the Quartus Prime software version 15.1.1.

DisplayPort IP Core

- Fixes an issue where the HBR Dual and HBR Quad HSSI Native PHY presets for the Arria V and Stratix® V DisplayPort protocols have incorrect transmitter (TX) physical medium attachment (PMA) division factors. This fix includes the following modifications:
  - Updates the **DisplayPort_HBR_Dual.qprs** and **DisplayPort_HBR_Quad.qprs** Native PHY presets for Arria V and Stratix V IP variants.
  - Changes the `tx_pma_clk_div` setting from 2 to 1.

  This issue affects the Quartus Prime Standard Edition software.
- Removes audio support for the 2 symbols per clock configuration on Stratix V devices. This change in support affects the Quartus Prime Standard Edition software.
- Includes a design example that supports Arria 10 10AX115 ES3 and production device revisions.
- Updates the target device number associated with the Arria 10 design example from 10AX115S2F45I1SG to 10AX115S3F45E2SGE3.

EMR Uploader IP Core

- Updates the IP to include Arria 10 support, allowing the IP to handle all error detection cases.
- For Arria 10 EMR Uploader IP, fixes the clock cycle calculation on wait time for the second `CRCERROR` pulse.

EMIF IP

- For MAX 10 EMIF IP, enhances the calibration algorithm to ensure that the EMIF sequencer is able to center to the available working window when testing for data matches. This change affects the Quartus Prime Standard Edition software.
- For Arria 10 EMIF IP, fixes an issue that causes incorrect simulation results when using Abstract PHY to perform a QDR IV simulation.
- For MAX 10 EMIF LPDDR2 IP, revises the timing analysis script to match silicon result. This revision affects the Quartus Prime Standard Edition software.
- Includes a legality check in the Arria 10 EMIF IP for HPS that detects illegal pin configuration and identifies the affected pins. This legality check ensures that the pin configuration follows the pin placement restrictions on HPS EMIF pins that are used as FPGA GPIOs. For more information, refer to the **Knowledge Database**.
- Fixes an issue where the Quartus Prime software misplaces the Arria 10 EMIF IP for HPS in the wrong bank when the IP is in x32 or x16 mode. With this fix, the Quartus Prime software now issues an error message when the IP is misplaced. This issue affects Arria 10 SX devices where x64 and x70 models of the EMIF IP are available.

HDMI IP Core

- Updates the Arria 10 design example to support the Bitec HDMI 2.0 FMC Revision 4 daughtercard.
- Updates the Arria 10 design example to support the Bitec HDMI 2.0 HSMC Revision 8 daughtercard.

  Note: This updated design example is not compatible with Revision 2 daughtercards.
- Includes an HDMI design example that supports Arria 10 10AX115 ES3 and production device revisions.
- Updates the HDMI design example to support Arria 10 10AX115S3F45E2SGE3 devices.

HSSI IP Core

- For Arria 10 designs, implements the following PMA RBC changes:
  - Updates the GT receiver channel default values for `vga_sel`, `dc`, and `ac` gain settings.
  - Limits the receiver (RX) decision feedback equalization (DFE) capacity to greater than 4.5 gigabits per second (Gbps) data rates only.
  - Updates the `sd_threshold` setting for PCIe.
  - Updates the frequency limits for the Physical Coding Sublayer (PCS) Direct mode.
- Removes a false path and solves a potential timing failure on the `rate_sw` signals in PIPE Gen2 and PIPE Gen3 designs that target Arria 10 speed grade 2 and speed grade 3 devices.

  Note: PIPE Gen3 designs have an additional restriction. Do not place the designs over hard IP channels in speed grade 2 and speed grade 3 devices.
- Includes the following Arria 10 HSSI Calibration Code updates:
  - Updates power regulator calibration for clock network voltage levels up to 1.03 V and 1.12 V to match the updated Vccer/Vccet voltage levels.
  - Updates Charge Pump and duty cycle distortion (DCD) calibration to fix an issue that occurs during the recalibration of simplex channels.
  - Updates decision feedback equalization (DFE) calibration to start DFE and freeze all DFE taps after 100 ms.
  - Updates fPLL calibration to overcome a potential locking issue in fractional mode.

JESD204B IP Core

- Sets multicycle paths for quasi-static signals in the TX control and RX control modules.

Low Latency Ethernet 10G MAC IP Core

- Addresses the following issues in the IP parameter editor GUI:
  - Adds the hyperlink to the *Low Latency Ethernet 10G MAC User Guide*.
  - Corrects the display name for the Arria 10 GX Transceiver Signal Integrity Development Kit.

Low Latency 40GBASE-KR4 Ethernet PHY IP Core

- Updates Arria 10 IP for improved reliability and better backplane performance.

PCI Express Hard IP Core

- Fixes an issue where the Arria 10 PCIe hard IP fails to properly set the `rxpolarity` PIPE control on a given lane if this lane gains symbol lock (that is `rxvalid=1`) after the IP has started receiving TS2 ordered sets in the Polling.Active state.

  Attention: This fix adds to the PCIe polarity inversion fixes addressed in **IP and IP Cores** on page 13.
- Updates the ATX PLL analog settings in PCIe Gen3 mode for Arria 10 devices.
- Includes a new hidden parameter (`enable_skp_det`) in the PCIe GUI. Enabling `enable_skp_det` instantiates additional logic in the Arria 10 PCIe hard IP core to detect SKP errors.
- Updates the TX Equalization Preset 10 value for Arria 10 PCIe hard IP.
- For Arria 10 PCIe hard IP, disables the VF count check to allow the use of SRIOV-2 bridge in multiphysical function mode where VF has a value of 0.
- For Arria 10 PCIe hard IP, fixes an incorrect legality check that compares protocol data rate versus device speed grade.

Serial Digital Interface II IP Core

- Updates the reconfiguration management module to resolve an issue that occurs when Arria 10 TX PHY and RX PHY within the same channel need to operate independently.

Altera SDK for OpenCL

Attention: Unless stated otherwise, the following Altera SDK for OpenCL issues are associated with both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

- Fixes an internal exception error that might occur when the only predicated instruction within an OpenCL kernel is a store instruction.
- Fixes an internal exception error that might occur when the value of a variable exceeds the acceptable range.
- Fixes a rare internal exception error in the Altera Offline Compiler that might occur during a memory optimization pass.
- Fixes a Windows-only runtime issue, where the number and size of kernel arguments might cause the Altera SDK for OpenCL to invoke a kernel that targets a Stratix V device with incorrect arguments. This issue is associated with the Quartus Prime Standard Edition software.

Issues Addressed in Update 1

Quartus Prime Standard Edition Software

Quartus Prime Device Support

- For MAX 10 devices with a single power supply, enhances support for designs with output pins that you assign with the following I/O standards:
  - Dedicated RSDS
  - External RSDS - RSDS_E_3R
- Updates Arria 10 HSSI calibration code.
- For Arria 10 devices, enables the clock data recovery (CDR) unit to use lower voltage-controlled oscillator (VCO) frequencies to service common data rates. Lower VCO frequencies translate to reduced power consumption.
- For Arria 10 devices, optimizes an advanced transmit phase-locked loop (ATX PLL) voltage regulator setting.
- Changes the adaptation start sequence in TTK to allow more control by the uC.
- Adds Serial Flash Loader support for Arria 10 10AS066E2 and 10AX066E2 devices.
- Disables the x16 deep mode for Stratix V memory logic array block (MLAB) design with Byte Enable because the Quartus Prime Standard Edition software does not support this configuration.
- Enables the programming file for Arria 10 10AX066E2 and 10AS066E2 devices.

Quartus Prime Compilation and Design Flows

- Updates I/O buffers, routing wires, and clock networks in the Arria 10 timing models.
- Enhances the routing algorithm for Arria 10 devices.
- Fixes an issue that might cause an error during simulation script generation when a Quartus Prime project includes Quartus Prime IP Files (**.qip**) that you create.
- Updates Arria 10 SoC bitstreams to support the early release feature of the hard processor system (HPS)-shared I/O bank after I/O configuration shift register (IOCSR) programming.

- Fixes an issue that prevents the JTAG USERCODE value from being programmed into MAX 10 devices because the JTAG USERCODE value is not stored in the Programmer Object File (**.pof**). With this fix, the JTAG USERCODE value selected for a MAX 10 design is stored in the **.pof** file and is programmed into the device.
- Fixes an issue that prevents the JTAG USERCODE value from being programmed into Arria 10 devices because the JTAG USERCODE value is not stored in the SRAM Object File (**.sof**). With this fix, the JTAG USERCODE value selected for an Arria 10 design is stored in the **.sof** file and is programmed into the device.
- Fixes timing model errors related to the HPS Ethernet MAC and the internal HPS clock network. This issue affects Arria 10 SoCs.
- Fixes an issue in the Assignment Editor, where the filter bar fails to filter a node name with a fixed string if the string contains special characters such as ":" or "|".
- For Arria 10 10AX115 ES, 10AX066 ES, and 10AS066 ES devices, enables you to set a Quartus Prime Settings File (QSF) assignment that overrides the transmitter (TX) termination default value.
- Updates the height calculation for contour mode eyes in the Transceiver Toolkit to account for possible asymmetry.
- Fixes an issue where the number of HSSI channels shown in the Chip Planner is less than the number of HSSI channels stated in the Arria 10 device datasheet.

Quartus Prime Programmer

- Reduces programming time for MAX 10 10M02 devices.
- Updates the beta version of the QCrypt Arria 10 bitstream encryption tool to release version 1.1. Version 1.1 of the encryption tool allows additional security options to be set on the command line and enhances the security of encrypted designs. Previous beta version of the QCrypt tool is now deprecated.
- Fixes a non-volatile key programming issue for the Arria V, Cyclone V, and Stratix V device families.

Fitter

- Fixes an internal error that might occur when running `SPECTRAQ_PHYSICAL_SYNTHESIS` on a design containing `set_location_assignment` directives that lock a look-up table (LUT) or flipflop to a specific lab location. Prior to this fix, the internal error was prone to occur in the Altera SDK for OpenCL (AOCL) compilation flow with Partial Reconfiguration because AOCL used the `set_location_assignments` directives internally.
- For Arria V, Arria 10, Cyclone V, and Stratix V designs, fixes an issue that might cause the Fitter to insert an extra register on the `byte-enable` port of Fitter-created MLAB blocks, which leads to an extra cycle of delay. This issue only affects RAM blocks that are set to **Auto** for type and use the `byte-enable` port, which the Fitter automatically converts to MLAB blocks. This issue does not affect RAM blocks that are directly instantiated as MLAB blocks.
- For Arria 10 designs that use the Transceiver PHY Reset Controller IP, fixes an internal error in the Fitter when you enable the **Performance (High effort)** or the **Spectra-Q Physical Synthesis** compiler setting.
- Adds an optimization that might reduce Fitter run time for Arria 10 designs that contain many `set_max_skew` timing constraints. This optimization only affects designs that are compiled with the new TimeQuest Timing Analyzer timing algorithms enabled by default for Arria 10 devices.
- Updates the Fitter to perform EMIF I/O legality check during automatic I/O pin placement. In addition, fixes an issue where the Fitter produces a fit with illegal pin locations without issuing an error, but errors out when you back annotate the pin placement. This issue occurs when the EMIF IP is used and the placement of I/O pins is almost full. With this fix, the software checks the legality rules for every I/O pin during placement, including both auto-assigned and user-assigned pin locations. This issue affects MAX 10 10M16, 10M25, and 10M50 devices.

- Fixes an abnormal exit at the end of the Fitter stage of compilation. The abnormal exit occurs when an Arria 10 design contains Altera LVDS components and specifies migration devices.
- Fixes an issue where performing device migration using MAX 10 devices might cause an internal error in the Fitter.
- Fixes the check that ensures a location assignment made by user constraints does not exceed the HSSI tile level resource limit. Prior to this fix, the malfunctioning check resulted in wrong resource conflicts. This issue affects designs that target Stratix V devices.
- Modifies the Fitter's DSP packing for Arria V, Cyclone V, and Stratix V devices to avoid potentially incorrect behavior that involves merging DSP cells using scan-chain connectivity. Prior to this modification, the incorrect behavior was not detected until post-fit simulation.
- Fixes an internal error that might occur in the Fitter when you enable the `SPECTRAQ_PHYSICAL_SYNTHESIS` compiler setting and then compile a design containing a signal that exits a partition and then immediately reenters the same partition (that is, the signal creates a loop-back path around the same partition).
- Fixes the delay on the negative terminal of the true differential buffer. Prior to this fix, the delay might have an incorrect negative value, causing the Quartus Prime software to error out. This issue affects Arria 10 devices.
- For Arria 10 designs, fixes an issue where the Quartus Prime software might place two cascaded I/O PLLs in different I/O columns, causing an internal error in the Fitter.

Quartus Prime Pro Edition Software

Quartus Prime Software Installation

- Fixes an issue where the Nios® II Command Shell, installed with the Quartus Prime Pro Edition software, fails to launch. This fix directs the Nios II Command Shell setup script to search the ***<nios2eds_root_install>*/../quartus/bin64** directory for Quartus Prime binaries.

Quartus Prime Device Support

- Updates Arria 10 HSSI calibration code.
- For Arria 10 devices, enables the clock data recovery (CDR) unit to use lower voltage-controlled oscillator (VCO) frequencies to service common data rates. Lower VCO frequencies translate to reduced power consumption.
- For Arria 10 devices, optimizes an advanced transmit phase-locked loop (ATX PLL) voltage regulator setting.
- Changes the adaptation start sequence in TTK to allow more control by the uC.
- Adds Serial Flash Loader support for Arria 10 10AS066E2 and 10AX066E2 devices.
- Enables the programming file for Arria 10 10AX066E2 and 10AS066E2 devices.

Quartus Prime Compilation and Design Flows

- Fixes an internal error that might occur when preserving the placement of a portion of a compiled Arria 10 design.
- Addresses the following synthesis issues:
  - Fixes an issue where signed shifters with a negative shift amount might be synthesized incorrectly.
  - Fixes an issue where assignments to registers outside if-posedge-clock blocks might be processed incorrectly.
- Fixes an internal error that occurs when compiling an Arria 10 design that contains external memory interfaces and Partial Reconfiguration partitions.
- Updates I/O buffers, routing wires, and clock networks in the Arria 10 timing models.

- Enhances the routing algorithm for Arria 10 devices.
- Fixes an issue that might cause an error during simulation script generation when a Quartus Prime project includes Quartus Prime IP Files (**.qip**) that you create.
- Updates Arria 10 SoC bitstreams to support the early release feature of the hard processor system (HPS)-shared I/O bank after I/O configuration shift register (IOCSR) programming.
- Fixes an internal error that might occur when using the BluePrint Platform Designer and certain IP cause name collisions during synthesis.
- Fixes an issue that prevents the JTAG USERCODE value from being programmed into Arria 10 devices because the JTAG USERCODE value is not stored in the SRAM Object File (**.sof**). With this fix, the JTAG USERCODE value selected for an Arria 10 design is stored in the **.sof** file and is programmed into the device.
- Fixes timing model errors related to the HPS Ethernet MAC and the internal HPS clock network. This issue affects Arria 10 SoCs.
- Fixes an issue in the Assignment Editor, where the filter bar fails to filter a node name with a fixed string if the string contains special characters such as ":" or "|".
- For Arria 10 10AX115 ES, 10AX066 ES, and 10AS066 ES devices, enables you to set a Quartus Prime Settings File (QSF) assignment that overrides the transmitter (TX) termination default value.
- Updates the height calculation for contour mode eyes in the Transceiver Toolkit to account for possible asymmetry.
- Fixes an issue where the number of HSSI channels shown in the Chip Planner is less than the number of HSSI channels stated in the Arria 10 device datasheet.

Quartus Prime Programmer

- Updates the beta version of the QCrypt Arria 10 bitstream encryption tool to release version 1.1. Version 1.1 of the encryption tool allows additional security options to be set on the command line and enhances the security of encrypted designs. Previous beta version of the QCrypt tool is now deprecated.

Fitter

- Fixes an internal error that might occur when running `SPECTRAQ_PHYSICAL_SYNTHESIS` on a design containing `set_location_assignment` directives that lock a look-up table (LUT) or flipflop to a specific lab location. Prior to this fix, the internal error was prone to occur in the Altera SDK for OpenCL (AOCL) compilation flow with Partial Reconfiguration because AOCL used the `set_location_assignments` directives internally.
- For Arria 10 designs, fixes an issue that might cause the Fitter to insert an extra register on the `byte-enable` port of Fitter-created MLAB blocks, which leads to an extra cycle of delay. This issue only affects RAM blocks that are set to **Auto** for type and use the `byte-enable` port, which the Fitter automatically converts to MLAB blocks. This issue does not affect RAM blocks that are directly instantiated as MLAB blocks.
- For Arria 10 designs that use the Transceiver PHY Reset Controller IP, fixes an internal error in the Fitter when you enable the **Performance (High effort)** or the **Spectra-Q Physical Synthesis** compiler setting.
- Adds an optimization that might reduce Fitter run time for Arria 10 designs that contain many `set_max_skew` timing constraints. This optimization only affects designs that are compiled with the new TimeQuest Timing Analyzer timing algorithms enabled by default for Arria 10 devices.
- Fixes an abnormal exit at the end of the Fitter stage of compilation. The abnormal exit occurs when an Arria 10 design contains Altera LVDS components and specifies migration devices.
- Fixes an issue that causes the Fitter to encounter congestion on a global signal that is routed only to partition destinations. This issue might affect routing of a `CLKUSR` calibration signal to one or more Altera HSSI IP cores.

- Fixes an internal error that might occur in the Fitter when you enable the SPECTRAQ_PHYSICAL_SYNTHESIS compiler setting and then compile a design containing a signal that exits a partition and then immediately reenters the same partition (that is, the signal creates a loop-back path around the same partition).
- Fixes the delay on the negative terminal of the true differential buffer. Prior to this fix, the delay might have an incorrect negative value, causing the Quartus Prime software to error out. This issue affects Arria 10 devices.
- For Arria 10 designs, fixes an issue where the Quartus Prime software might place two cascaded I/O PLLs in different I/O columns, causing an internal error in the Fitter.

IP and IP Cores

Attention: Unless stated otherwise, the following IP issues apply to both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

Altera IOPLL IP Core

- For Arria 10 IOPLL IP, enables the **PLL Auto Reset** parameter setting when the IOPLL reset soft IP workaround is used. The **PLL Auto Reset** feature automatically self-resets the PLL on loss of lock.
- Fixes a usability issue by specifying the name of the PLL in the illegal generic PLL error message.
- Updates the Arria 10 IOPLL IP so that IP generation errors out if the IOPLL has more than seven output counters while the **PLL Auto Reset** feature is enabled.
- Fixes an issue related to the PLL_CTR_RESYNC parameter on the altera_pll module. This issue causes failures during VHDL simulation of designs targeting Arria 10 devices.

Altera On-Chip Flash IP Core

- Addresses the following MAX 10 On-Chip Flash IP core issues that affect the Quartus Prime Standard Edition software:
  - Improves timing for parallel mode by pipelining the arclk and ardin signals.
  - Fixes an issue in parallel and serial modes to prevent the IP from locking up when a write operation or an erase time-out operation occurs.

Altera PHYLite IP Core

- Suppresses the following warning message, which appears during the Fitter and timing analysis stages of a Quartus Prime compilation when the Arria 10 IOPLL soft IP workaround is enabled:

```
warning: derive_pll_clocks was called multiple  times with different options.
repeated calls to derive_pll_clocks do not  modify existing clocks.
```

Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core

- Removes undesired false path assignments in the IP and applies new constraints in the clock crossing paths. After you apply this update, regenerate the IP and use the resulting IP Synopsys Design Constraints File (**.sdc**). In addition, remove the constraints under the False Path within PHY section because they are no longer necessary.
- Refreshes the reconfiguration data to match latest clock data recovery (CDR) updates.

Arria V Ethernet 10GBASE-R PHY 1588 IP Core

- Adds RTL and SDC updates to improve timing closure for clock domain crossing paths. This issue affects the Quartus Prime Standard Edition software.

Arria 10 fPLL IP Core

- Enables the fPLL IP to correctly interpret values of L that you specify at the command line during IP generation.

DisplayPort IP Core

- Fixes design errors in the Arria 10 design example that cause errors during the Fitter stage of a Quartus Prime compilation.
- Fixes an error in the Arria V DisplayPort Multi-Stream design example that causes a compilation failure. This issue affects the Quartus Prime Standard Edition software.
- For Arria V and Stratix V design examples, updates the XCVR Reset Component Megawizard file to use the correct device. This issue affects the Quartus Prime Standard Edition software.
- Resolves a timing violation in the Arria 10 design example.
- Adds new DisplayPort Multi Stream Transport (MST) 4 streams design example for Stratix V devices. This issue affects the Quartus Prime Standard Edition software.

EMIF IP

- For Arria 10 EMIF IP, extends the dynamic termination signal for on-chip termination (OCT) earlier at higher frequencies. This update ensures that there is sufficient time to fully enable OCT before the IP receives read data.
- Suppresses the following warning message, which appears during the Fitter and timing analysis stages of a Quartus Prime compilation when the Arria 10 IOPLL soft IP workaround is enabled:

```
warning: derive_pll_clocks was called multiple  times with different options.
repeated calls to derive_pll_clocks do not  modify existing clocks.
```

- Fixes an issue that causes EMIF calibration to fail when two memory interfaces share a tile that contains address or command pins.
- Adds support for I/O PLL merging and I/O PLL duplication between Arria 10 EMIF interfaces when the I/O PLL workaround is enabled.
- Updates the I/O PLL jitter values in Arria 10 EMIF designs that run with a VCO frequency lower than 600 MHz.
- Improves Arria 10 EMIF calibration algorithm. This improvement resolves potential `vref-out-write-deskew` calibration failure of DDR4 high-speed interfaces. For non-DDR4 protocols, this improvement enhances window centering during write deskew by using a more complex training pattern.
- Fixes false recovery timing violations at user reset inputs. With this fix, Arria 10 EMIF IP's user reset output (`emif_usr_reset_n`) is now correctly associated with the EMIF user clock (`emif_usr_clk`).
- Fixes an issue in the Tcl script that is used for Arria 10 EMIF Abstract PHY simulation.
- Implements a mechanism to ensure that the EMIF interface releases from reset before the NIOS II-based sequencer performs calibration.
- For DDR2, DDR3, and LPDDR2 SDRAM, fixes an issue that causes incorrect timing constraints, resulting in timing violations for memory cores in MAX 10 devices. This issue affects the Quartus Prime Standard Edition software.

FIFO IP Core

- Fixes an issue where the Error Checking and Correction (ECC) parameter or port is missing for the mixed_width_dcfifo simulation model. In addition, adds the `eccstatus` output port and the `enable_ecc` parameter in the simulation model.

HDMI IP Core

-]Fixes a design flaw that causes the IP to fail CTS testing under the 4 symbols per clock configuration.
- For the Arria 10 HDMI Video IP design example, fixes an issue that might cause functional failure when the IP is used with fPLL.

HPS IP Core

- Fixes an issue where Arria V SoC or Cyclone V SoC ignores the PLL User Clock 2 frequency that you set in Qsys for the HPS IP component and uses the default value instead. With this fix, the Quartus Prime Standard Edition software correctly applies the selected PLL User Clock 2 setting in the HPS.
- Fixes an issue where the HPS erroneously tries to configure some of the I/O pins as HPS pins when the HPS EMIF is not used and the I/O interface next to the HPS is made available to the FPGA. This issue has no effect if the HPS EMIF is used.
- Fixes an issue where the HPS AXI issuance and issuance specifications that the HPS IP component generates in the Qsys conduit exceed the support limit of the silicon. Prior to this fix, this issue caused minor performance degradation in the AXI interface. This fix includes the proper HPS AXI issuance and issuance specifications for optimal AXI performance.
- Fixes an issue where the HPS IP component incorrectly advertises to the Qsys fabric that the HPS FSDRAM AXI interface does not support data reordering. The HPS FSDRAM AXI interface supports data reordering and prior to this fix, this issue might cause erratic behavior in `rlast` signal assertion for burst lengths of 2 or 3.

HSSI IP Core

- Updates Arria 10 transceiver VCCR and VCCT power supply levels from 0.9 V to 0.95 V and from 1.11 V to 1.12 V.
- Addresses the following issues for Arria 10 HSSI IP:
  - Adds warnings for the Transceiver Reset Controller core for the **rx_analogreset duration** and **tx_digitalreset duration** fields. The warnings appear when these fields have a value less than 70 µs.
  - Modifies the **Arria 10 Default Settings** preset to set the **TX digital reset mode** to **Auto**.
  - Modifies the **Default Settings** preset to specify a default value of 0 for the **tx_analogreset duration** field.
- For Arria 10 HSSI IP, adds a legality check to ensure that TX `posttap1` is set before setting `posttap2`. In addition, updates a legality check for the maximum limit on GT transceiver data rates.
- For Arria 10 HSSI IP, fixes an issue where the resource calculation engine does not count the `rx pin as refclk` pin as an HSSI channel when performing resource calculation for an HSSI tile. Prior to this fix, when a `rx pin as refclk` pin was locked to an HSSI tile, it prevented you from using the CDR PLL that was at the same HSSI channel.

JESD204B IP Core

- Resolves a critical warning on unused transceiver receiver (RX) channels for the JESD204B design example.

Low Latency Ethernet 10G MAC IP Core

- Removes the embedded false path in the DCFIFO that the non-1588 Arria 10 design example uses. Prior to removing the embedded false path, packet corruption might occur in the design example if the FIFO mode was set to DCFIFO.

Low Latency 40- and 100-Gbps Ethernet MAC and PHY IP Cores

- Fixes an issue in the low latency 100Gbps Ethernet MAC IP where the IEEE 1588 precision time protocol interface function might misbehave in rare cases. This issue affects Arria 10 devices.
- Corrects the clock names in the **.sdc** file for the low latency 40Gbps Ethernet IP hardware design example targeting Arria 10 devices.
- Addresses the following Ultra-Low Latency 100G Ethernet IP issues:
  - Adds a synchronizer in the MAC Status Register to prevent a clock domain-crossing issue.
  - Adds RX physical coding sublayer (PCS) firmware to periodically check for frame error condition in order to prevent the IP from locking up.

LVDS SERDES IP Core

- Suppresses the following warning message, which appears during the Fitter and timing analysis stages of a Quartus Prime compilation when the Arria 10 IOPLL soft IP workaround is enabled:

```
warning: derive_pll_clocks was called multiple  times with different options.
repeated calls to derive_pll_clocks do not  modify existing clocks.
```

PCI Express Hard IP Core

- Fixes a functional issue regarding polarity inversion in PCI Express (PCIe). This fix enables the option for PCIe hard IP to use both static inversion and dynamic inversion.
- Implements an RX polarity inversion soft logic to fix an Arria 10 PCIe hard IP RX polarity issue. The soft logic is enabled via the hidden `rx_polinv_soft_logic_enable` parameter, which is disabled by default. The soft logic performs the following functions:
  - Reconfigures the Avalon Memory-Mapped (Avalon-MM) master to enable the `rx_dyn_polinv` bit setting of the PHY after the FPGA fabric is active.
  - Detects inverted `rx_ts2` and set the `pld_rx_polinv`.

Serial Digital Interface II IP Core

- Changes clock multiplier unit (CMU) settings in the Arria 10 SDI II design example to select a valid output frequency for CMU.
- Resolves transceiver warning in the SDI multi-rate (up to 12G) RX preset and enables the `tx_pma_div_clkout` port for the SDI multi-rate (up to 12G) TX preset in order to obtain the 148.5 MHz clock for the protocol.
- For the SDI II Video IP, fixes an issue where a sync bit that is not inserted on ancillary data might affect the operations of other SDI components, particularly in the 6G-SDI and 12G-SDI modes.

SerialLite III Streaming IP Core

- Fixes an issue that might cause a Fitter error in an Arria 10-specific SerialLite III simplex source design with the ECC parameter enabled.
- For designs that run in tethered mode, removes timeout limit for OpenCore Plus. This issue affects the Quartus Prime Standard Edition software.

DSP Builder Advanced Blockset

- Adds support for MATLAB Simulink's **Comment Through** feature. Enabling the **Comment Through** feature for a block or a subsystem allows signals to pass through the block or subsystem, which does not appear in the synthesized design.

  This **Comment Through** feature support applies to both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

Altera SDK for OpenCL

Attention: Unless stated otherwise, the following Altera SDK for OpenCL issues are associated with both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

- Fixes a functional issue that might occur in rare cases when an OpenCL design has several control flow segments that are merged during a branch conversion optimization.
- Fixes an Altera Offline Compiler (AOC) loop analysis issue where the AOC misidentifies a value as a loop-carried dependency, which causes functional incorrectness. Prior to this fix, the issue manifested as a variable in a nested loop that used an incorrect initialization value on subsequent initial iterations of the loop.
- Reduces the maximum number of devices that the Altera Runtime Environment (RTE) for OpenCL for Cyclone V SoCs can accommodate from 32 to 16 in order to reduce memory consumption. This issue is associated with the Quartus Prime Standard Edition software.
- Reduces static memory requirements for AOCL host programs running on Cyclone V SoCs. This issue is associated with the Quartus Prime Standard Edition software.
- Fixes an internal exception issue in the AOC that might occur in rare cases during memory optimization.
- Fixes an issue in the AOC that might cause hardware generation to fail when you attempt to unroll a loop that uses channels.
- Fixes an internal exception issue in the AOC that occurs when memory dependence analysis asserts in cases where there is a mismatch in the address computation types.
- Fixes a fatal error that results in the following message: `Assertion `isConditional() && "Cannot get condition of an uncond branch!" failed.` This error might occur in designs with infinite loops that perform initial data preprocessing outside of the loop.
- Fixes a fatal error that results in the following message: `ERROR: Port/Signal [ffwd_25_0] already exists!` This error might occur in single work-item kernels and high-level synthesis (HLS) designs.
- Fixes an internal exception issue in the AOC that occurs when the logic that controls the loop pipelining control signals are placed in stall-free regions within the datapath. This issue might incorrectly create an assertion in rare cases.
- Fixes an internal exception issue in the AOC that might occur when you use uncommon integer sizes in an HLS design.
- Fixes an internal exception issue that might occur when a design has a misalignment of constant loads.
- Fixes an internal exception issue that might occur when a design has two paired loop bounds whose ranges are being analyzed and they have an offset of 1.
- Fixes an internal exception issue that might occur when a design has a basic block that is always false.
- Fixes a fatal error that results in the following message: `Running pass 'Module Verifier' on function '@response_whitelist_filter'. Error: Optimizer FAILED.` This error might occur when the kernel source code has unreachable code sections.
- Fixes an internal error that might occur in Arria 10 designs that rely on Partial Reconfiguration.

JNEye

Attention: Unless stated otherwise, the following JNEye issues are associated with both the Quartus Prime Standard Edition software and the Quartus Prime Pro Edition software.

- Improves the accuracy of the Arria 10 receiver model and fixes an issue in the Channel Designer GUI.
- Fixes an issue with the IBIS-AMI statistical simulation engine where it occasionally misinterprets the transmitter amplitude effect.

Software Issues Resolved

Table 1: Customer Service Requests Resolved in the Quartus Prime Design Suite Version 15.1 Update 2

Customer Service Request Numbers Resolved					
11134872	11181936	11186227	11187335	11188484	11189055
11192531	11193000	11193218	11194317	11195377	11198286
11198614	11198724	—	—	—	—

Table 2: Customer Service Requests Resolved in the Quartus Prime Design Suite Version 15.1 Update 1

Customer Service Request Numbers Resolved					
11172256	11174046	11174561	11176925	11178254	11178580
11179841	11179862	11180764	11181819	11182416	11183059
11183538	11184929	11186288	11186567	11187172	11187890
11188039	11188268	11188631	11189502	11190201	11190573

Software Patches Included in Update Releases

Table 3: Software Patches included in the Quartus Prime Design Suite 15.1 Update 2

Software Version	Patch	Customer Service Request Number
Quartus Prime 15.1.1	1.01	—
Quartus Prime 15.1.1	1.02	—
Quartus Prime 15.1.1	1.03	—
Quartus Prime 15.1.1	1.06	—

Table 4: Software Patches included in the Quartus Prime Design Suite Version 15.1 Update 1

Software Version	Patch	Customer Service Request Number
Quartus Prime 15.1	0.12	11172256
Quartus Prime 15.1	0.08	11181819
Quartus Prime 15.1	0.07	11176925

Software Version	Patch	Customer Service Request Number
Quartus Prime 15.1	0.04	11187172
Quartus Prime 15.1	0.01	—
Quartus II 15.0.2	2.17	11181819
Quartus II 15.0.2	2.16	11174561
Quartus II 15.0.2	2.15	11174046
Quartus II 13.0	0.59	11180764

Known Issues and Workarounds

This section provides information about the following known issues that affect the Quartus Prime software version 15.1.

Description	Quartus Prime Edition Affected	Workaround
If you use Google Chrome to load locally-installed Quartus Prime Help, you might be prompted to disable some JavaScript functionality.	Standard and Pro	For the best viewing experience using Google Chrome, navigate to **http://quartushelp.altera.com/current/index.htm** to access Quartus Prime Help. For more workaround options, refer to the **Altera Knowledge Database**.

For information about known software issues, please visit the Altera Knowledge Database.

Related Information

- **Altera Knowledge Database**
- **Altera Documentation: Release Notes**
- **Quartus Prime and Quartus II Software Support**

Document Revision History

Table 5: Quartus Prime Design Suite Version 15.1 Updates Document Revision History

Date	Document Version	Changes
February 2016	2016.02.22	Added Quartus Prime Design Suite version 15.1 update 2 information.
December 2015	2015.12.14	Added Quartus Prime Design Suite version 15.1 update 1 information.