# Altera Complete Design Suite Version 15.0 Update Release Notes

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This version of the *Altera® Complete Design Suite Update Release Notes* describes the Altera Complete Design Suite version 15.0 software update 2.

The Altera Complete Design Suite version 15.0 software update requires the Altera Quartus® II software release version 15.0. If you do not have the Quartus II software release version 15.0, please install it prior to installing any Altera Complete Design Suite version 15.0 software updates to ensure the Quartus II software runs properly.

Altera Complete Design Suite updates are cumulative; Update 2 includes Update 1.

**Related Information**

**Quartus II Software and Device Support Release Notes Version 15.0**

## Issues Addressed in Update 2

### Quartus II Software Installation

- Fixes an issue in the Quartus II software version 15.0.1 where the installation process incorrectly installs some files as symbolic links.

### Quartus II Device Support

- Enables physics-based I/O placement legality checks for MAX® 10 FPGAs, and updates parasitic data for 10M02, 10M08, 10M16, 10M25, and 10M50 devices.
- Fixes an issue in Stratix® V GT device transceivers where the internal serial loopback debugging aid fails to work in Quartus II software versions 14.0 and later.
- Enables backward compatibility support for MAX 10 10M16 devices.
- Includes support for the Arria® 10 10AX115S2F45I1SGE2 device.
- Enables Quartus II software I/O Bank 1A and 1B support as two different banks for MAX 10 10M04, 10M08, 10M16, 10M25, 10M40, and 10M50 devices. You may use this I/O bank under the following conditions:
  - You can enable the analog-to-digital converter (ADC) in I/O Bank 1A (MPS: 2.5, SPS: 3.0/3.3V) and JTAG in I/O Bank 1B (1.5V to 3.3V, with the reference voltage (VREF) pin unused).
  - You can supply separate $V_{CCIO}$ voltages to Bank 1A and 1B, provided that the VREF pin is unused.
  - You must supply the common $V_{CCIO}$ voltage to both I/O Bank 1A and 1B when the VREF pin is used.
- Includes Programmer Object File (**.pof**) support for MAX 10 10M25 devices.



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# Quartus II Compilation and Design Flows

- Fixes an error that affects specific designs, where the error prevents the PowerPlay Early Power Estimator (EPE) from completing the generation of a PowerPlay EPE file.
- Fixes a PowerPlay Power Analyzer issue, allowing it to run on MAX 10 Flash and analog-to-digital-converter (ADC) designs without causing a fatal error.
- Fixes the following issues in the Design Space Explorer II (DSE II):
  - Fixes a Windows-specific error, enabling the DSE II to use any free ephemeral network ports.
  - Fixes an issue where clock names containing "[", "]", "|", and other regular expression special characters are missing in the DSE II reports.
- Fixes an issue in the DSE II that occurs when you specify Load Sharing Facility (LSF) resource, priority, and environment variable settings in the GUI or from the command line.
- Fixes an issue in the Quartus II software Convert Programming File tool to allow the generation of a Programmer Object File (**.pof**) in **Passive Parallel x8** mode. This issue affected Stratix IV, Cyclone® IV, and Arria II devices.
- Fixes an integer overflow issue that causes an internal error when compiling designs that use certain fractional phase-locked loop (fPLL) configurations.
- Fixes an issue where timing models for Arria V FPGAs and Arria V SoCs (except Arria V GZ devices) have miscorrelated timing paths in some Core-to-Periphery (C2P) data paths. Refer to the **Altera Knowledge Database** for more information.
- Fixes a Pin Planner display error for 36-pin and 81-pin Very FineLine Ball-Grid Array (VBGA) packages. This error affected MAX 10 devices. For more information, refer to sample PCB routing schemes on 36-pin and 81-pin VBGA packages in *Designing with High-Density BGA Packages for Altera Devices*.
  - **Sample PCB Routing Scheme on 4 Layers for 0.4-mm 81-pin VBGA**
  - **Sample PCB Routing Scheme on 2 Layers for 0.4-mm 36-pin VBGA**
- Fixes an issue that causes the incorrect labeling of valid values in the Transceiver Toolkit.

## Fitter

- Fixes a Cyclone IV device-specific issue in the Fitter report when the receiver uses external transmitter termination. Prior to the fix, the misleading message `OCT 100 Ohms` appeared in the Fitter I/O pin report. After the fix, when external termination is enabled, the message `External Termination` appears in the Fitter report. Otherwise, it reports the actual on-chip termination (OCT) resistance in ohms (for example, `OCT 150 Ohms`).
- Fixes an internal error that occurs when some usages of carry chains within the logic array block (LAB) are falsely detected as invalid. With this fix, you can now use these legal configurations in your design. This issue affected designs targeting Arria 10 devices.
- For designs targeting MAX 10 10M16, 10M25, and 10M50 devices, adds a legality check to prevent the generation of an invalid Programmer Object File (**.pof**) when both of the following conditions are satisfied:
  - You use a fast input register in a dual-input mode design.
  - You assign the fast input register into I/O Bank 5 and I/O Bank 6.
- Fixes an issue that causes long compilation times on Linux platforms when you do not set the *NUM_PARALLEL_PROCESSORS* variable in your Quartus II Settings File (**.qsf**).
- Fixes an internal error that might occur when you enable the Physical Synthesis feature and then compile a Stratix V design.

# DSP Builder Advanced Blockset

- Fixes an issue that causes the `DSPBA_Features.alwaysBreakOffMemRegs` flag to generate incorrect hardware for finite impulse response (FIR), numerically controlled oscillator (NCO), and cascaded integrator-comb (CIC) blocks.
- Fixes an issue within the logic that implements the Avalon® Memory-Mapped (Avalon-MM) slave interface for DSP Builder Advanced Blockset (DSPBA) designs. Prior to the fix, the `readdatavalid` signal in the read response path was asserted unexpectedly, causing the Avalon-MM master to retrieve data from the DSPBA Avalon-MM slave when the request was addressed to a different slave.

# IP and IP Cores

## DisplayPort IP Core

- Enables the OpenCore Plus hardware evaluation feature.
- Fixes a compilation error by adding a parameter condition when the DisplayPort source **Maximum lane count** parameter (`TX_MAX_LANE_COUNT`) in the **bitec_dp_tx_skew.v** module is set to 1 lane.
- Includes missing files in the hardware demonstration **make** file so that you can generate a functional example design.
- Fixes a linking issue in the example design when the source and the sink have different resolution capabilities.

## HDMI IP Core

- Fixes an issue that occurs when you run Arria V and Stratix V device-specific example designs for lower video resolutions at data rates lower than 600 megabits per second (Mbps).
- Fixes an interoperability issue that occurs when the IP core interfaces with certain models of monitors and TVs.
- Enhances the Arria V and Stratix V example designs to demonstrate the deep color capability on the 2 symbols per clock configuration for 8, 10, and 12 bits per color.
- Fixes an issue where the IP core fails to compile in Windows because of the end-of-line character in the Synopsys Design Constraints File (**.sdc**) generated in Linux.

## HPS IP Core

- Introduces a critical warning issued by the Quartus II software when you enable the HPS early release feature for the Arria 10 SoC engineering sample (ES) device.
- Includes the following changes for the Arria 10 SoC HPS:
  - Fixes an issue that prevents the HPS Light Weight Advanced eXtensible Interface (AXI) bridge from disabling properly. This issue occurs when the HPS Light Weight bridge is enabled in the Arria 10 SoC HPS and the HPS Light Weight AXI bridge in the Qsys HPS IP component is disabled.
  - Adds a warning message that appears if the L3 free clock divider for the Arria 10 SoC HPS has a **Divide by 2** configuration in the Qsys IP component. Altera recommends that you always configure the L3 free clock divider setting to **Divide by 4**.

## Interlaken PHY IP Core

- Fixes an issue that prevents you from updating the IP core using the **Upgrade IP Components** dialog box.

### PCIe Hard IP

- Fixes a timing closure violation issue when using the Arria 10 HIP root port (RP).

### SDI Audio IP

- Fixes an issue that occurs during Audio Extract IP core generation when the Avalon Streaming (Avalon-ST) interface is disabled.

### SerialLite III Streaming IP Core

- Updates IP example design for Stratix V devices to fix a timing violation.

### Soft LVDS IP Core (MAX 10 Devices)

- Fixes an issue where the `tx_outclock` and `tx_coreclock` frequencies are incorrect for odd serializer/deserializer (SERDES) factors.

## Altera SDK for OpenCL

- Fixes a functional incorrectness that occurs in designs with initiation interval (II) values higher than 50. Prior to this fix, this issue caused discrepancies between kernel functionality and emulation results.
- Fixes an assertion issue that occurs as a result of loop pipelining-related optimizations.
- Fixes an internal error that occurs as a result of local memory optimizations.
- Increases host runtime device support from 16 devices to 32 devices.
- Adds OpenCL™ Shared Virtual Memory (SVM) application programming interface (API) support to emulation.

# Issues Addressed in Update 1

## Quartus II Software Installation

- Fixes an issue that causes the installation of a design template to fail when the path to the destination directory contains a space.

## Quartus II Device Support

- Includes support for 92 new Arria 10 devices.
- Updates MAX 10 device LVDS differential output voltage ($V_{OD}$) setting options to include 0 (low), 1 (medium) and 2 (high).
- Adds a PCI clamp diode option for MAX 10 devices with a 2.5V or 3.3V Schmitt trigger input buffer setting.
- Discontinues support for the MAX 10 10M08DAF484C7G device. Altera recommends the MAX 10 10M08DAF484C8G device as a replacement.
- Includes Programming Object File (**.pof**) support for MAX 10 10M16 devices.

## Quartus II Compilation and Design Flows

- Fixes an issue that prevents the **Report Routing Utilization** dialog box from appearing in the Chip Planner when a design fails in the compilation routing stage.
- Replaces an internal error with a user error that describes the problem. The error occurs when your design targets an Arria 10 10AX115 device and you lock a logic array block (LAB) with too many inputs into a region that does not have enough resources to support the inputs.
- Adjusts the maximum vertical step value in the Transceiver Toolkit EyeQ feature for Arria 10 devices.
- Fixes an issue in designs targeting Arria 10 devices, where certain timing constraints that use the `-through` option with wildcards cause an internal error in the Fitter (`quartus_fit`).
- Fixes the IP Catalog to reduce IP search times. Prior to the fix, in some cases, the IP Catalog took a long time to perform a search and the Quartus II software was unresponsive for the duration of the search.
- Fixes an issue that causes an internal error in the Fitter. This issue affected designs targeting Arria 10 devices.
- Fixes an issue that causes Continuous Time Linear Equalization (CTLE) adaptation in the Transceiver Toolkit to fail for a specific Arria 10 device configuration.
- Fixes an issue that disables the start button in the Transceiver Toolkit EyeQ feature. This issue affected designs targeting Arria 10 devices.
- Fixes an issue that causes the Storage Qualifier feature of the SignalTap™ II Logic Analyzer to miss samples.
- Fixes an issue where clock names containing "[", "]", "|" and other regular expression special characters are missing in the Design Space Explorer II reports.
- Fixes an issue that causes timing violations in some designs targeting Arria 10 ES devices.
- Fixes an issue that causes the PowerPlay Power Analyzer to generate an internal error when using the Arria 10 3V I/O power model.

  **Note:** Arria 10 I/O power models are preliminary.
- Fixes an error that occurs in MAX 10 I/O power models.
- Fixes the Design Space Explorer II, allowing it to use any free ephemeral network ports in Windows.

## Quartus II Programmer

- Reduces the amount of time required for an Arria 10 device to enter user mode after device configuration.
- Fixes an issue that causes device configuration to fail when using the ASCII text-based Jam™ Standard Test and Programming Language (STAPL) file (**.jam**) or the byte-code Jam STAPL file (**.jbc**) to configure a MAX 10 device that has a blank on-chip flash memory.
- Fixes an issue that causes JTAG chain programming to fail if you have a MAX 10 device in a JTAG chain and you attempt to bypass the MAX 10 device and program another device in the chain. This fix allows you to bypass the MAX 10 device in a JTAG chain without interruption.
- Includes an enhancement that speeds up the programming time of a MAX 10 device.
- Enables the following Stratix V parts in the Programmer:
  - 5SEEBH40I3YY
  - 5SEEBF45I3YY
  - 5SGSMD4E3H29I3YY
  - 5SEEBF45I3YY
  - 5SGXEB6R3F40I3YY
  - 5SGXEA7K3F35I3YY

- Fixes an issue that causes the JTAG Chain Debugger tool to generate an internal error when testing the integrity of a JTAG chain, if the JTAG chain contains an Altera device that does not support USERCODE instruction.
- Fixes an issue that causes the Fault Injection Debugger tool to generate an internal error when evaluating some designs that target Arria 10 devices.
- Updates the `quartus_cvp` executable by extending the read timeout for the configuration status registers after certain Configuration via Protocol (CvP) configuration operations complete.

## Fitter

- Fixes an Arria 10 device-specific issue that causes physical synthesis optimizations in the Fitter to incorrectly merge two registers with different timing exceptions, such as false paths or multicycle paths.
- Fixes an issue that causes an internal error to occur when an Arria 10 device design satisfies both of the following criteria:
  - Includes two or more digital signal processing (DSP) blocks that use an 18x18 multiplication mode.
  - The input and output registers do not use the same pair of clock and clock enable signals.
- Fixes a legality check issue in the Quartus II software version 15.0 that causes an abnormal exit during the Fitter stage when the `listen_to_nsleep_signal` parameter is set to `true` but the `nsleep` port is not connected. Prior to this fix, if your design targeted a MAX 10 10M16, 10M25 and 10M50 devices and you used an input buffer atom, or used Altera's general-purpose I/O (GPIO) Lite IP core to construct your IP, the Quartus II software might trigger an abnormal exit instead of generating a user error.
- Fixes an issue that erroneously allows MAX 10 device designs to use nonexistent connectivity between `DPCLK` pins and the clock network.
- Fixes an issue that causes an internal error in the Fitter when a carry chain for an Arria 10 device has no data input except for the carry-out signal from above and the first carry-in signal is grounded.
- Improves the ability of the Fitter to optimize designs that use certain types of long wires to achieve timing closure.
- Fixes an issue that unnecessarily constrains the fractional phase-locked loop (fPLL) that is driving the high-speed serial interface (HSSI) channel through the core clock. Prior to this fix, an internal error occurred when you performed the second Fitter run with all the location constraints from the first run and some of the fPLLs were not located on the same strip as the corresponding HSSI channels. This issue affected designs targeting Stratix V, Cyclone V, Arria V and Arria 10 devices.
- Improves optimization of placement and routing of Arria 10 designs, particularly for high-speed pipelined designs.
- Amends the following Physics I/O placement rule parameter data:
  - Crosstalk factor
  - EQFP package parasitic data for MAX 10 10M08, 10M16, 10M25 and 10M50 devices
- Fixes an issue that causes an internal error in the Fitter when a design uses one or more `CLOCK_REGION` Quartus Settings File (**.qsf**) assignments.

## Qsys

- Optimizes how Qsys version 15.0 handles the propagation of the `SYSTEM_INFO` address map between Avalon Memory-Mapped interface (Avalon-MM interface) masters and their corresponding slaves. Prior to the fix, in some cases, Qsys took a long time to load and validate systems with IP cores that used Avalon-MM master interfaces.

# IP and IP Cores

### 16550 UART IP

- Fixes circular buffer formula errors in the IP to prevent data overflow and to prevent data from being overwritten.

### 40- and 100-Gbps Ethernet MAC and PHY IP Cores

- For Arria 10 low-latency IP core variations, includes system console example design test scripts in the **example_project/hwtest** directory.
- Updates KR4 link training algorithm for Arria 10 low-latency IP core variations. This change also updates the control and status registers (CSR) definitions and modifies the default values for the 0xd0 register in these IP cores.
- Fixes an issue in the KR4 reconfiguration bundle that causes reconfiguration into the Autonegotiation mode to fail if temperature-based Decision Feedback Equalizer (DFE) tuning is active. This issue affected the Stratix V IP core variations.

### Advanced SEU Detection IP Core

- Enables support for Arria 10 devices. Refer to the **Altera Advanced SEU Detection IP Core User Guide** for more information about the IP core.

### Altera General-Purpose I/O Lite IP Core (ALTERA_GPIO_LITE)

- Fixes an issue where the Qsys-generated ModelSim® script (**msim_setup.tcl**) is missing the MAX 10 device family library information. This issue affected all MAX 10 designs that used the **msim_setup.tcl** script to run simulation in ModelSim.

### ALTGX-RECONFIG IP Core

- Fixes an issue in Quartus II software versions 14.1 and 15.0, where the insertion of incorrect adaptive look-up table (ALUT) atoms occurs when the number of channels controlled by the `reconfig` controller exceeds the following values:
  - Six for Arria II GX/GZ devices
  - Four for Cyclone IV GX devices
  - Six for Stratix IV devices

### Arria 10 1G/10G PHY and 10GBASE-KR PHY IP Cores

- Updates the link training algorithm. This change also updates the CSR definitions and modifies the default values for the 0x4d0 register in these IP cores.
- Updates link training algorithm. This change also fixes an issue where the CSR bit 0x4d2[0] register does not reflect the correct value when you test your design in hardware.

### Arria 10 Transceiver ATX PLL IP Core

- Fixes an issue that causes the IP reconfiguration process to generate an incomplete Memory Initialize File (**.mif**) when dynamic reconfiguration for the ATX PLL IP core is enabled. If you enable ATX PLL dynamic reconfiguration and use IP-generated **.mif** files, update the ATX PLL IP to version 15.0.1.

### EMIF IP

- Enables the voltage and temperature compensation feature in MAX 10 IP variations.
- Optimizes the quad data rate IV (QDR-IV) soft memory controller in Arria 10 IP variations to improve timing closure.
- For Arria 10 IP variations, fixes a GUI issue that causes the **ODT Activation Settings** tab to disappear when switching memory protocol.
- Fixes an issue that causes the Hardened Processor Subsystem to lock up when performing byte-oriented accesses to the external SDRAM while the error correction code (ECC) circuitry is enabled. This issue affected the Arria 10 10AS057 and 10AS066 devices.

### FIR II IP Core

- Enables noninteger input rates and allows the generation of the simulation file set. Prior to this update, noninteger input rates caused version 15.0 of the IP compiler GUI to fail.

### JESD204B IP Core (Arria 10 devices)

- Corrects the `PMA_WIDTH` setting. The incorrect `PMA_WIDTH` setting caused the JESD SoftPCS Variant Example Design simulation to fail.

### HDMI IP Core

- Corrects the RTL that causes a timing violation on the `*mr_rx_oversample:RX_OVERSAMPLE*` path when you run the example design in the ***<IP root directory>*/altera/altera_hdmi/hw_demo/av_sk_hdmi2** directory.

### HPS IP Core

- Fixes an issue that affects designs targeting Arria V SoC and Cyclone V SoC, where timing analysis identifies the wrong timing violations in the HPS F2SDRAM Bridge when a design uses multiple F2SDRAM ports that are connected to multiple clock domains. With this fix, you can now generate a Synopsys Design Constraints (SDC) file that produces the correct timing report for the F2SDRAM Bridge.
- Includes the following changes for the Arria 10 HPS IP core:
  - Fixes routing congestion issues that arise when HPS Advanced eXtensible Interface (AXI) bridges are in use. This fix also improves the $F_{max}$ of AXI bridges by 5% and reduces the compilation time when HPS AXI bridges are in use.
  - Adds a warning message that notifies you of known issues with the HPS SDMMC power enable polarity pin.
  - Enables the HPS SDMMC 1-bit mode.
- Fixes an issue that occurs during RTL generation of the HPS F2SDRAM in Qsys, causing the HPS F2SDRAM AXI bridge to fail in your IP.

### RapidIO IP Core (Arria 10 Devices)

- Fixes an issue that makes ambiguous reference to the `alt_xcvr_resync` module when you instantiate the Transceiver Reset Controller that is generated with the RapidIO IP core.

  **Attention:** If you instantiate the Transceiver Reset Controller generated with the IP core, you must change the input clock frequency at the top-level wrapper file. If you generate a new Transceiver Reset Controller from the IP Catalog, no action is necessary.

### PCIe Hard IP

- Fixes an issue in the PCI Express® (PCIe®) Hard IP that uses the Avalon-MM interface, allowing you to access the Data Link Layer Active Reporting (`dll_active_report_support_hwtcl`) and Surprise Down Error Support (`surprise_down_error_support_hwtcl`) configuration space options from the user interface and modify their settings.
- Fixes an issue that happens when running the Avalon-MM direct memory access (DMA) interface in hardware, where a DMA data mismatch failure occurs after performing a DMA upstream write. This issue affected PCIe Hard IP in Stratix V devices that use external memory such as DDR3.
- Fixes an issue that causes a Quartus II compilation error when you configure PCIe as the Root Port device with a 64-bit Avalon-MM interface.

### Transceiver IP Cores (Arria 10 Devices)

- Updates the default values for **Transmitter Slew Rate**. The Quartus II software now generates an updated default setting for **Transmitter Slew Rate** if the Arria 10 transmitter channels do not have Assignment Editor (or **.qsf**) settings for it.

### Transceiver Native PHY IP Core (Arria 10 Devices)

- Fixes an issue that causes one of two Simplex IP sharing the same Native PHY channel to fail during the reconfiguration of the other Simplex IP. The IP creation process generates a reconfiguration file. Before this fix, if two IP (e.g. TX and RX) shared the same Native PHY channel and you streamed in the data from the reconfiguration file during TX reconfiguration, the data also changed the settings of RX and caused it to fail.

### Video and Image Processing Suite IP Cores

- Includes OpenCore Plus support.

### Virtual JTAG Megafunction IP Core

- Fixes an issue with the the SLD_VIRTUAL_JTAG_BASIC megafunction IP core, allowing the proper use of the `sld_auto_instance_index` HDL parameter.

## Altera SDK for OpenCL

- Fixes an internal error in the Altera Offline Compiler (AOC), where in rare cases, the AOC generates illegal hardware when `if` conditions in a kernel program merge together with memory accesses.

## Simulation and Synthesis

- You can use the simulation scripts to automate compilation and simulation of all Altera IP in a design, along with any test bench, test programs, and other simulation content. The Quartus II software v15.0.1 introduces a new method to generate and combine individual simulation scripts generated for each Altera IP core in your design. This new method produces a single simulation script that does not require manual update for upgrades to Quartus II software or IP versions.

  The new `ip-setup-simulation` utility finds Altera IP cores in a Quartus II project, and runs the existing `ip-make-simscript` utility to generate a combined script. `ip-setup-simulation` also automates regeneration of a combined IP simulation script following upgrade of the Quartus II or IP core version.

  **Attention:** If you use the simulation script, run this utility after upgrading ACDS or IP cores.

  For more information about this feature, refer to **Altera Knowledge Database**.
- Fixes an issue introduced in the Quartus II software version 14.0, where the names of some combinational nodes in the top hierarchy are in the form of `rtl-<n>`, instead of synthesized names that are based on the logic in the original hierarchy. Prior to this fix, nodes with names `rtl-<n>` were excluded from LogicLock™ regions that recognized hierarchical names.

## SoC Embedded Design Suite

- Fixes an issue with the Embedded Design Suite (EDS) Flash Programmer (`quartus_hps`), allowing queued serial peripheral interface (QSPI) programming to take into account the system clock frequency when you set the clock frequency for the QSPI controller. This issue affected designs targeting Arria 10 SoCs.

# Software Issues Resolved

**Table 1: Customer Service Requests Resolved in the Altera Complete Design Suite Version 15.0 Update 2**

| Customer Service Request Numbers Resolved | | | | | |
|---|---|---|---|---|---|
| 11129370 | 11145297 | 11147700 | 11150442 | 11152131 | 11153517 |
| 11155346 | 11157606 | — | — | — | — |

**Table 2: Customer Service Requests Resolved in the Altera Complete Design Suite Version 15.0 Update 1**

| Customer Service Request Numbers Resolved | | | | | |
|---|---|---|---|---|---|
| 11092459 | 11106729 | 11116930 | 11118549 | 11119286 | 11122259 |
| 11136037 | 11137683 | 11139661 | 11140401 | 11140716 | 11141157 |
| 11141905 | 11148302 | 11149692 | 11148436 | — | — |

# Software Patches Included in Update Releases

**Table 3: Software Patches included in the Altera Complete Design Suite Version 15.0 Update 2**

| Software Version | Patch | Customer Service Request Number |
|---|---|---|
| Quartus II 15.0 | 0.17 | — |
| Quartus II 15.0 | 0.23 | — |
| Quartus II 15.0.1 | 1.01 | — |
| Quartus II 15.0.1 | 1.06 | — |

**Table 4: Software Patches included in the Altera Complete Design Suite Version 15.0 Update 1**

| Software Version | Patch | Customer Service Request Number |
|---|---|---|
| Quartus II Arria 10 Edition 14.1 | 0.08sa | — |
| Quartus II 14.1.1 | 1.13 | — |
| Quartus II 14.1.1 | 1.16 | 11148436 |
| Quartus II 15.0 | 0.07 | 11106729 |
| Quartus II 15.0 | 0.10 | — |
| Quartus II 15.0 | 0.16 | — |

# Latest Known Altera Complete Design Suite Issues

For information about known software issues, please visit the Altera Knowledge Database.

**Related Information**

- Altera Knowledge Database
- Altera Documentation: Release Notes
- Quartus II Software Support

# Document Revision History

**Table 5: Altera Complete Design Suite Version 15.0 Updates Document Revision History**

| Date | Document Version | Changes |
|---|---|---|
| July 2015 | 15.0.2.0 | Added Altera Complete Design Suite version 15.0 update 2 information. |
| June 2015 | 15.0.1.0 | Added Altera Complete Design Suite version 15.0 update 1 information. |