Altera Complete Design Suite Version 14.1 Update Release Notes

January 2015

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This version of the *Altera® Complete Design Suite Update Release Notes* describes the Altera Complete Design Suite version 14.1 software update 1.

The Altera Complete Design Suite version 14.1 software update requires the Altera Quartus® II software release version 14.1. If you do not have the Quartus II software release version 14.1, please install it prior to installing any Altera Complete Design Suite version 14.1 software updates to ensure the Quartus II software runs properly.

Related Information

Quartus II Software and Device Support Release Notes Version 14.1

Issues Addressed in Update 1

Quartus II Device Support

- Includes support for the following MAX® 10 devices:
  - 10M04SAU169C8G
  - 10M04SCU169C8G
  - 10M04SFU169C8G
  - 10M08SAU169C8G
  - 10M08SCU169C8G
  - 10M08SFU169C8G
  - 10M16SAU169C8G
  - 10M16SCU169C8G
  - 10M16SFU169C8G
  - 10M25SAE144C8G
  - 10M40SAE144C8G
  - 10M50SAE144C8G
- Improves the timing models for MAX 10 10M40 and 10M50 devices, providing more accurate clock delays.
- Includes final pinout support for MAX 10 10M16 devices.
- Includes vertical migration support from the MAX 10 10M02 device to the 10M08 device.

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- Updates the MAX 10 FPGA bit settings for single power supply (SPS) devices to improve the analog-to-digital converter (ADC) performance.
- Enables the error detection cyclic redundancy check (EDCRC) feature for the MAX 10 single-power supply device. To prevent functional failures when running your design on a single-power supply device, a critical warning message will remind you to run the PowerPlay Early Power Estimator (EPE) file to ensure your design is within the maximum power utilization limit of the target device.
- Includes software support for the Cyclone® IV EP4CE55F23A7 device.

Quartus II Compilation and Design Flows

- Fixes the IP Catalog, allowing it to update when you change search paths to support the addition of IP cores to your project.
- Fixes an issue that causes the ADC Toolkit to fail if the service path name includes spaces.

Quartus II Programmer

- Fixes an issue with the cascaded multi-device FPPx16 configuration mode on Arria® V devices.

Fitter

- Fixes an issue that causes the Fitter to fail and generate the following error when you use the import and export design partition features in your MAX 10 device design:

```
Error: Found x UFM blocks in design -- only one UFM block is allowed.
Error: Found x ADCBLOCK blocks in your design, however your device can only
accommodate one ADCBLOCK block.
```

- Fixes the LVDS I/O placement rule to enable noise calculation for all I/O bank pins in use. Prior to this fix, an internal error occured in the Fitter if you migrated your design from MAX 10 10M08/10M50 devices to 10M16/10M02/10M25 devices.
- Fixes an issue that causes the Fitter to generate an internal error when an external memory interface (EMIF) debug component is connected to two or more EMIF IP components on an Arria 10 device.
- Fixes an issue that occurs when multiple EMIF IP components are placed in an I/O column on an Arria 10 device, but only some of the IP components have pin constraints. The issue causes the Fitter to generate an internal error.
- Includes a LVDS transmit (TX)/ receive (RX) package skew compensation report for the Arria 10 device.

Qsys

- Fixes `CLOCK_RATE`, allowing Qsys to correctly propagate clock rate values to children of composed IP components.

IP and IP Cores

100-Gbps Ethernet MAC and PHY IP Core (Legacy)

- Fixes the example design for custom client interface variations so the example compiles successfully.

Altera On-Chip Flash IP Core

- Fixes an initialization issue that causes the Quartus II software to incorrectly interpret the initialization file content when the initialization file has insufficient data.
- Corrects the configuration flash memory (CFM) address mapping in the IP core. Prior to this fix, the CFM address mapping was incorrect for all MAX 10 compact (C) devices, except the 10M02 device.

ALTERA_FP_FUNCTION IP Core

- Fixes an issue that causes the scalar product to map to soft logic, even when targeting hard digital signal processing (DSP) blocks.

ALTERA_MULT_ADD IP Core

- Fixes an IP upgrade failure error that occurs during IP component upgrade.

HPS IP Core

- Adds the correct `h2f_` suffix to the Arria 10 hard processor system (HPS) interrupt signals to match the standard HPS interface names.
- Fixes an issue that affects designs targeting Cyclone V SoCs, where the lower limit of the external crystal oscillator frequency is set to 125 MHz; you can now select frequencies from 1 MHz to 125 MHz for the HPS user 0 clock.
- The HPS FPGA to SDRAM interface port F2SDRAM2 is not available for the Arria 10 ES device. You must use the F2SDRAM0 and F2SDRAM1 ports, or select another device.
- Disables the HPS F2SDRAM2 Advanced eXtensible Interface (AXI) Bridge for Arria 10 ES devices; this interface is not available in ES silicon.

MAX 10 EMIF IP

- Fixes a hardware functional issue by increasing the UniPHY Dual-Clock FIFO (DCFIFO) buffer depth and Data Valid Prediction FIFO (VFIFO) buffer length for MAX 10 devices.

RapidIO IP Core (Arria 10 Devices)

- Fixes a licensing error in the IP core; prior to this fix, an invalid license warning message would generate during the Assembler stage.

Transceiver Native PHY IP Core (Arria 10 Devices)

- Fixes an Avalon Memory-Mapped (Avalon-MM) high-speed serial interface (HSSI) issue that occurs when the interface is not shared. Prior to this fix, if the Arria 10 Transceiver Native PHY IP core had an independent dynamic reconfiguration interface for each channel, any write operations to Channel 0 would propagate to the other channels, and any write operations to the other channels would write incorrectly.
- Corrects the port name corresponding to the **Enable rx_pma_qpipulldn port (QPI)** parameter in the GUI to `rx_pma_qpipulldn`. Prior to this fix, the port name was erroneously displayed as `rx_pma_qpipullup`. If your Arria 10 Native PHY IP design enables this port, you must update your design to use the new port name.

Transceiver Native PHY IP Core (Stratix V Devices)

- Includes support for the slowest speed grade (4_H3).

Triple Speed Ethernet, Custom PHY, and Transceiver Native PHY IP Cores

- Fixes an issue where HSSI clocks (for example, `rx_pma_clkout`) connecting to periphery clocks are stuck to 0 for Cyclone V D9 devices.

DSP Builder Advanced Blockset

- Fixes an issue that causes the generate stage of the system-in-the-loop flow to exit with an unsatisfied dependency error.
- Fixes an issue with the scheduler to restore the expected quality of results (QoR) for multi-subsystem designs. Prior to this fix, the scheduler incorrectly placed registers at the outputs to meet timing for designs with more than one subsystem.
- Improves the support for complex signals on the BitCombine block, allowing DSP Builder to generate hardware with the same behavior as the simulation model. Prior to this fix, Simulink simulation would work, but DSP Builder failed when hardware generation was enabled.
- Fixes an issue that causes DSP Builder to crash MATLAB when you open a DSP Builder design, created in version 13.1 or earlier, in the 14.1 release. Prior to this fix, any design using the Resource Sharing Folder caused a MATLAB system error when you enabled hardware generation and ran a simulation.

Nios II Embedded Design Suite

- Fixes an issue where the Nios® II board support package (BSP) generation fails with an error reporting the electrically programmable configuration quad-serial (EPCQ) driver does not support the enhanced interrupt application programming interface (API). Prior to this fix, the error occured when the Nios II processor used an external interrupt controller (EIC) and was attached to the Altera Serial Flash Controller (`altera_epcq_controller`).

Altera SDK for OpenCL

- Adds Nallatech's p385_hpc_a7 board to the list of offline devices.
- Fixes an issue where the Altera Offline Compiler (AOC) fails to generate hardware in Windows systems if the Quartus II software and Qsys tools are not in your *PATH* environment variable.
- Fixes an assertion in the AOC; prior to this fix, the optimizer could fail during compilation.
- Fixes Verilog generation functionality; prior to this fix, the kernel could hang when running hardware.
- Fixes an issue where emulator runs produce incorrect results or crash under certain circumstances due to a data race in the emulator runtime. The issue occurs for some combinations of task and NDRange kernels. Prior to this fix, successive identical runs of emulated host + kernel might produce incorrect results.
- Fixes an internal loop pipelining bug; prior to this fix, the module verifier could crash.
- Enhances performance to leverage specific on-chip RAM characteristics, ensuring loop-carried dependencies achieve a maximum throughput. Pipelined loops can still use an initiation interval of one cycle (in other words, the loops are perfectly pipelined).
- Fixes an issue where the OpenCL™(1) software development kit (SDK) compiler generates incorrect hardware or internal errors for some applications when the board support package (BSP) has 1 or 4 channels of memory.
- Fixes an issue that causes memory dependence analysis to crash.
- Fixes an internal assertion in the compiler, where in rare cases, the compiler generates invalid instruction sequences. Prior to this fix, the optimizer failed when you declared a float type in a `pow` function.
- Improves emulator compile time from the previous software release.

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- Fixes an internal bug that affects initiation interval (II) estimation in single-threaded kernels.
- Corrects the license information text to the correct version; prior to this fix, the 14.1 OpenCL **license.txt** referenced software version 14.0.
- Fixes register promotion and shift register inference for cases where you declare an array with a size defined by a constant variable. Your code now works with either form of declaration:

```
#define N ...
int normal[N];
const int n = ...
int now_works[n];
```

- Fixes an AOC driver error that occurs when you use `--profile` and relative paths are defined with `-I`
- Reduces the area overhead for nested loops.

Simulation and Synthesis

- Includes the Mentor Graphics® Precision synthesis tool that was erroneously missing from the Quartus II software version 14.1 **EDA Tool Settings**.
- Fixes an issue that causes the ModelSim®-Altera Starter Edition to request a license when no license is required.

Software Issues Resolved

Table 1: Customer Service Requests Resolved in the Altera Complete Design Suite Version 14.1 Update 1

Customer Service Request Numbers Resolved					
11062137	11085145	11094180	11096354	11100796	11103034
11109430	11109505	11109833	11112119	11112372	—

Software Patches Included in Update Releases

Table 2: Software Patches included in the Altera Complete Design Suite Version 14.1 Update 1

Software Version	Patch	Customer Service Request Number
ModelSim 14.1	0.01m	—
Quartus II 14.0	0.32	11094180
Quartus II 14.0.2	2.12	11094180
Quartus II 14.1	0.01	11062137
Quartus II 14.1	0.02	11085145
Quartus II 14.1	0.04	—
Quartus II 14.1	0.08	11094180

Latest Known Altera Complete Design Suite Issues

For information about known software issues, please visit the Altera Knowledge Database.

Related Information

- Altera Knowledge Database
- Altera Documentation: Release Notes
- Quartus II Software Support

Document Revision History

Table 3: Altera Complete Design Suite Version 14.1 Updates Document Revision History

Date	Document Version	Changes
January 2015	14.1.1.0	Added Altera Complete Design Suite version 14.1 update 1 information.