Altera Complete Design Suite Version 14.0 Arria 10 Edition Update Release Notes

2014.09.01

RN-01080-14.0Arria10.1.0 Subscribe Send Feedback

The Altera® Complete Design Suite version 14.0 Arria® 10 edition software updates require the Altera Quartus® II software release version 14.0 Arria 10 edition. If you do not have the Quartus II software release version 14.0 Arria 10 edition, please install it prior to installing any Altera Complete Design Suite version 14.0 Arria 10 edition software updates to ensure the Quartus II software runs properly.

Related Information

Quartus II Software and Device Support Release Notes Version 14.0 Arria 10 Edition

Issues Addressed in Update 1

Quartus II Compilation and Design Flows

- Fixes an internal error that occurs when you launch the Technology Map Viewer (Post-Fitting) with a design using memory logic array blocks (MLABs).

Qsys

- Removes recommended upgrade messages from Qsys. Prior to this fix, you could erroneously receive recommended IP upgrade notifications when your IP versions were up-to-date.
- Includes new messages relating to version compatibility and upgrading of the following IP cores:
  - alt_em10g32
  - alt_pr
  - altera_eth_tse
  - altera_jesd204
  - altera_rapidio
  - altera_rapidio2
  - altera_xcvr_fpll_a10
  - altera_xcvr_native_a10
  - altera_xcvr_xaui
  - sdi_ii

IP and IP Cores

- Fixes an issue causing incorrect or missing version numbers for IP included in your design from a Qsys System File (.qsys) or Quartus II IP File (.qip). This fix also corrects a segmentation fault in the IP identification code.
- **HPS IP**
  - Corrects the order of the hard processor system (HPS) component pins `HPS_DIRECT_SHARED_Q1_1` to `HPS_DIRECT_SHARED_Q4_12` for the Arria 10 10AS066 and 10AS057 devices in the Quartus II software and Qsys. The HPS pin functions were numbered incorrectly in the Quartus II software release version 14.0 Arria 10 edition. After installing the Altera Complete Design Suite version 14.0 Arria 10 edition update 1, you must regenerate your Arria 10 HPS I/O design to correct the HPS pin placements.
  - Fixes a trace port interface unit (TPIU) component issue to correct pin connections and assignments. Prior to this fix, when you enabled the trace interface Qsys placed any unconnected trace pins in an I/O region not included in the shared HPS I/O region, and the Quartus II software instantiated your design with 3 of the 4 trace data pins (`TRACE_D`) disconnected. Any Arria 10 HPS IP design using the TPIU in the CoreSight™ debug component requires this fix.
  - Fixes an issue that prevents the Quartus II software from correctly displaying the flow control pins for the HPS IP component in Qsys. Prior to this fix, if you selected the flow control pins, the pins did not update correctly in the main or advanced tabs of the pin multiplex GUI.
- **JESD204B IP Core**
  - Fixes the incorrect interface type of `jesd204_rx_int` and `jesd204_tx_int` to enable connection to interrupt receiver components in Qsys.
  - Fixes the signal type of `pll_locked`, `tx_cal_busy`, `rx_cal_busy` and `rx_is_lockedtodata` to resolve a signal type mismatch issue when connecting the IP core and the transceiver reset controller component in Qsys.
  - Fixes the `DEVICE_FAMILY` parameter's default value, enabling you to generate a JESD204B Qsys design using Qsys script commands.
- **LVDS SERDES IP Core**
  - Fixes a Synopsis Design Constraints (SDC) error when your SDC file has a virtual clock.
  - Fixes a SDC error when your design file uses VHDL with multiple hierarchies in the same file.
  - Changes SDC errors to critical warnings and improves the warning messages when external phase-locked loops (PLLs) are connected incorrectly.

Software Issues Resolved

Table 1: Customer Service Requests Resolved in the Altera Complete Design Suite Version 14.0 Arria 10 Edition Update 1

Customer Service Request Numbers Resolved					
11073969	—	—	—	—	—

Software Patches Included in Update Releases

There are no Quartus II software patches included in the Altera Complete Design Suite version 14.0 Arria 10 edition update 1 release.

Latest Known Altera Complete Design Suite Issues

Table 2: Latest Known Altera Complete Design Suite Version 14.0 Arria 10 Edition Update 1 Issues

Description	Workaround
The Quartus II software does not recognize an available update to the JESD204B IP core An optional upgrade is available for the JESD204B IP core in this release of the Altera Complete Design Suite. However, neither the IP Components window in the Project Navigator nor the IP Upgrade dialog box indicate that the upgrade is available.	To upgrade your IP, use the IP Parameter Editor for the JESD204B IP core. Automatic upgrade is not available. For information on features included in this optional upgrade, refer to the JESD204B IP Core section of **Issues Addressed in Update 1**.

For further information about known software issues, please visit the Altera Knowledge Database.

Related Information

- **Altera Knowledge Database**
- **Altera Documentation: Release Notes**
- **Quartus II Software Support**

Document Revision History

Table 3: Altera Complete Design Suite Version 14.0 Arria 10 Edition Updates Document Revision History

Date	Document Version	Changes
September 2014	Arria 10 Edition 14.0.1.0	Initial Release.