Altera Complete Design Suite Version 13.1 Update Release Notes

RN-01080-13.1.4.0 Release Notes

This document provides information about the Altera® Complete Design Suite Version 13.1 Update 4.

You must either have previously installed the Quartus® II software Version 13.1 or must install the Quartus II software version 13.1 before installing this update. Otherwise, the update will not be installed correctly and the Quartus II software will not run properly.

For information about the Quartus II software Version 13.1, refer to the *Quartus II Software and Device Support Release Notes Version 13.1*.

Altera Complete Design Suite updates are cumulative; Update 4 includes Updates 1 to 3.

Issues Addressed in Update 4

The Altera Complete Design Suite Version 13.1 Update 4 addresses the following software issues:

Altera SDK for OpenCL

- Fixes an Altera Offline Compiler (AOC) error that generated the message: `Assert failure at CreateStallFreeClusters.cpp(1287).`
- Fixes a cache size inference issue where the AOC could underestimate the OpenCL™ kernel cache size, which might lead to incorrect kernel functionality.
- Fixes an AOC error that generated the message: `Assert failure at InstrDataDep.cpp: Unsupported node with <node> outside cluster.`
- Enhances throughput of single work-item execution.
- Provides functional and deterministic fixes to ensure that, for a given OpenCL kernel source file, the AOC generates consistent outputs between compilations.
- Fixes a problem where incorrect hardware generation could cause a work-group to access local memory assigned to a different work-group.
- Updates the board package for the BittWare S5-PCIe-HQ Altera Stratix® V GSMD5 half-length PCI Express® (PCIe®) board, available with the Altera SDK for OpenCL Version 13.1, to match the board vendor-distributed S5-PCIe-HQ board package. The updated board package provides additional constraints to increase Configuration via Protocol (CvP) reliability.
- Updates the board package for the Nallatech PCIe-385N FPGA computing card, available with the Altera SDK for OpenCL Version 13.1, to include additional constraints to increase CvP reliability.

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- Addresses the following single work-item execution issues:
  - Enhances throughput and provides functional fixes to the single work-item kernels to maintain work-item execution order in the presence of channel instructions.
  - Fixes a functionally incorrect behavior that could occur when your single work-item kernel replicates local memory to relax memory dependencies.
- Addresses the following emulation and execution issues:
  - When creating context in the host program, you do not need to provide a print notification callback for printing error messages during emulation.
  - Fixes an issue with work-item execution order.
  - Automates emulation flow so that you do not need to include the `-ldl` flag in your `aocl` command to compile the host program for executing emulated kernels.
- Prevents the AOC from creating hardware instructions that the Altera SDK for OpenCL cannot process during hardware generation.

Quartus II Compilation Flows

- Fixes an issue in which, during compilation, the Quartus II software failed to find a postfit node in the postfit netlist for a clock source node with a name containing the `~inputCLKENA0` postfix. In the Signal Tap II Logic Analyzer Node Finder, with the SignalTap II: post-fitter filter enabled, if you selected such a node to be an acquisition clock, the SignalTap II Logic Analyzer grounded the corresponding input port connecting to the clock, resulting in no data acquisition.
- Fixes the following errors that could occur in the Quartus II software Version 13.1 after you updated it with the Altera Complete Design Suite Version 13.1 Update 3:
  - The **Convert Programming Files** dialog box might fail with a fatal error if you loaded a Conversion Setup File (**.cof**) file that you generated using an earlier version of the Quartus II software and then clicked **Properties** to open the **SOF Data Properties** dialog box.
  - When you invoked the command `quartus_cpf -c <filename>.cof` to generate files from **.cof** files, the error message `Error (213053): Device does not support design security` might appear.

    The conversion process generated valid output files despite the error message.
- Eliminates an internal error that could occur when you edited a symbol in the Block Editor.

Fitter

- For designs that target Arria® V GX A3 devices, fixes an issue that could cause an internal error because the Fitter assumed incorrect negative delays on the input path to a phase-locked loop (PLL).
- For designs that include PCIe Hard IP (HIP) cores with dummy channels, updates the Fitter behavior to ignore the dummy channels during placement legality checks.

Quartus II Programmer

- Enables you to generate backward-compatible Serial Configuration Device Programmer Object Files (**.pof**) using the Quartus II software Version 13.1 so that you can open them in the Quartus II software Versions 11.1 and earlier.

Qsys

- In the Qsys Hard Processor System (HPS) library module, updates the USB Controllers settings under the **Peripheral Pin Multiplexing** tab to support the single data rate (SDR) with PHY input clock mode.

Transceiver Toolkit

- Reduces memory usage by the Transceiver Toolkit when you run transceiver link tests in the combined Autosweep + EyeQ mode.

IP

Video and Image Processing IP

- Removes the Clocked Video Input II component from the list of available Video and Image Processing IP cores because the Quartus II software Version 13.1 does not support it.

Issues Addressed in Update 3

The Altera Complete Design Suite Version 13.1 Update 3 addresses the following software issues:

Device Support

- For Arria® V GZ devices, fixes an incorrect V_{CCIO} limitation for on-chip differential termination (R_D OCT).
- For Arria V SoC and Cyclone® V SoC devices, updates clock and routing delays to improve alignment with silicon.
- Sets final timing model status for the following devices:

Device Family	Device
Arria V SoC	5ASXB3
	5ASXB5
	5ASTD3
	5ASTD5
Cyclone V SoC	5CSEA2
	5CSEA4
	5CSEA5
	5CSEA6
	5CSXC2
	5CSXC4
	5CSXC5
	5CSXC6
	5CSTD5
	5CSTD6

Altera SDK for OpenCL

- Fixes the following floating-point operation and floating-point optimization issues:
  - Fixes a floating-point addition, subtraction, or multiplication operation support problem that could incorrectly flush a subnormal number result to zero instead of rounding it to the smallest normal number.
  - Fixes a problem with floating-point compiler (FPC) optimizations that could cause wide reduction operations (e.g. large adder trees) to consume large amounts of area unnecessarily.
- Fixes the following issues that could occur during memory dependence analysis:
  - Eliminates an internal error that could occur when an OpenCL™ kernel contains a non-constant memory dependence distance.
  - Fixes an issue that could cause the compiler to ignore loop-carried dependencies in load or store operations involving pointer arithmetic.

- Fixes an issue with excessive memory usage during compilation of an OpenCL kernel using the Quartus II software Version 13.1. .
- Addresses the following emulation issues:
  - Removes temporary files that could cause fatal errors to occur when iterating on emulation.
  - Improves the scalability of memory usage for a larger number of kernels.
  - Improves interactions between single work-item kernel programs and NDRange kernel programs.
  - Improves dynamic linking resolution for the Linux OpenCL host runtime library shared object (**.so**) files.
  - Improves simultaneous work-item execution.
  - Improves error reporting.
  - Includes support for vector channels.
- Reduces memory utilization when using the Quartus II software to compile the following OpenCL applications:
  - Designs that target BittWare S5P-HQ accelerator boards containing Stratix® V D5 or D8 devices.
  - OpenCL kernels that use file scope constant data arrays.
- Fixes a fatal memory access violation error that the Altera SDK for OpenCL runtime library might cause when your host program rapidly enqueues many short-running kernels.
- Addresses the following SoC-specific issues:
  - Upgrades the OpenCL SoC driver to support Linux kernel version 3.9.
  - Enables contiguous memory access optimizations for robust allocation of physically contiguous memory buffers.
  - Fixes an issue with the OpenCL SoC driver Makefile that generated an error when delivering the prebuilt `reprogram` utility.
- Addresses the following compilation issues:
  - Fixes Altera SDK for OpenCL Offline Compiler (AOC) compilation time issues.
  - Improves single work-item execution throughput.
  - Improves single work-item execution area usage.
- For an OpenCL kernel program that remains unchanged between compilations, corrects an issue where the AOC implemented optimizations that caused differences in the intermediate Verilog files it generated.

Quartus II Compilation Flows

- Fixes an issue where an optimization that generated a combinational loop might cause a fatal stack overflow error.
- For designs that target Stratix V, Arria V, or Cyclone V devices, addresses the following issues:
  - Fixes a problem that prevented the detection of illegal PCI Express® (PCIe®) Hard IP (HIP) hard reset pin location when other user location constraint errors existed. This fix allows the Quartus II software to report all illegal pin locations.
  - Enhances the legality check capability of the Quartus II software to prevent misinterpretations of legal HIP locations as errors.
- Allows you to save the following Design Security settings for each device when generating a Conversion Setup File (**.cof**):
  - Enables encryption options.
  - Key file specification.
  - Key selection.
- For designs that target Stratix V, Arria V, Arria V GZ, or Cyclone V devices, fixes an issue that could cause inefficient utilization and merging of phase-locked loop (PLL) resources, or suboptimal PLL placements.

Qsys

- For a design targeting Arria V GZ devices that includes a HIP for the PCIe Avalon® Memory-Mapped (Avalon-MM) bridge, fixes a Qsys system compilation error that occurred when generating a VHDL simulation system because the output `tlbfm_out` port was missing.

Simulation

- For a design simulation where you enable the **Enable physical output clock parameters** setting, fixes an issue that caused incorrect phase relationship between PLL output clocks and the reference clock because the voltage-controlled oscillator (VCO) period is indivisible by the M counter value.
- For VHDL simulations of designs that include the altera_pll and altera_pll_reconfig IPs, fixes an issue that generated an error message similar to the following:

```
# ** Error: Unresolved defparam reference to 'lcell_inst' in
lcell_inst.lut_mask.
# ** Error: Unresolved defparam reference to 'lcell_inst' in
lcell_inst.dont_touch.
```

Quartus II Programmer

- For Cyclone IV Serial Flash Loader (SFL) factory images that configure Cyclone IV E devices, fixes an issue that could cause some I/O pins serving as the JTAG-to-Active Serial interface bridge to drive low instead of maintaining their tri-state configurations.

SignalTap II Logic Analyzer

- Enhances the Data Log feature to include the following information:
  - Records in the name of the log the time at which a trigger action occurs.
  - Records in the name of the log the elapsed time between the start of acquisition and the occurrence of a trigger action.

Nios II EDS

- Adds Nios® II Software Build Tools (SBT) support for the interrupt request (IRQ) Bridge to record automatically in the **system.h** file the correct IRQs of components attached to an IRQ Bridge.

IP

- Fixes an erroneous behavior of the IP Upgrade dialog box where it notified you continuously that an upgrade for IP cores was available even after IP regeneration.

EMIF IP Cores

- Fixes an external memory interface calibration failure error in the hard processor system (HPS) preloader for Cyclone V SoC devices. This fix does not affect the external memory interface in the FPGA.

PLL IP

- For a design simulation where you enable the **Enable physical output clock parameters** setting and specify a **PLL Auto Reset** setting (i.e. **On** or **Off**), fixes an issue that always reverted the **PLL Auto Reset** setting back to its default value.
- For a design simulation where you enable the **Enable physical output clock parameters** setting and specify a **PLL Bandwidth Preset** setting, fixes an issue that always reverted the **Charge Pump and Bandwidth** setting back to its default value.

Issues Addressed in Update 2

The Altera Complete Design Suite Version 13.1 Update 2 addresses the following software issues:

Device Support

- Provides full compilation and programming support for the following Cyclone® V device: 5CGXFC5C6F23A7.
- Adds Serial Flash Loader support for the following Cyclone V devices: 5CSEA2, 5CSXC2, 5CSEA4, and 5CSXC4.
- Adds Hard Processor System (HPS) Loaner I/O timing support for Arria V SoCs and Cyclone V SoCs.

Qsys

- Fixes an issue that could cause incorrect information to be displayed in the Qsys Connections tab.
- For designs that target Arria V or Cyclone V SoCs, fixes an error that could prevent generation of Hard Processor System (HPS) Initial Software (**.isw**) files if a Quartus II IP file (**.qip**) assignment is in full path format. The error was:
  `Error (210006): Can't save or open file <filepath>/<filename>`

Quartus II Compilation Flows

- Fixes an issue that could cause incorrect logic implementation in DSP blocks if you select the input cascade feature for signals using DATAA_X, DATAA_Z, DATAB_X, or DATAB_Z.
- For designs that target Cyclone IV E, Cyclone IV GX, and Cyclone V devices, the Quartus II software now honors Pad-to-Core delay chain **.qsf** settings in the Strict Preservation flow.
- For designs that target Arria V devices, this update adds an optional **quartus.ini** setting to improve Arria V hold timing closure performance. To use this setting, add `tis_increase_fitter_hold_pessimism=ON` to your **quartus.ini** file, put the **quartus.ini** into your project directory, and then restart the Quartus II software.
- For designs that target a Stratix® V device, modifies a default setting on the Stratix V CDR/CMU PLL block, providing additional margin for when the device operates in cold temperatures.
- Eliminates an error that could occur during compilation of a design that targets and Arria V SoC or Cyclone V SoC, if the design uses both the hard processor system (HPS) and LVDS.
- Eliminates an internal error that could occur during compilation when a LAB is configured such that an SLOAD signal is placed on an input port designated for a different signal type.

- Eliminates an internal error that could occur in the Assembler when an I/O pin with `ENABLE_STRICT_PRESERVATION` is not connected to logic with compatible preservation settings. Instead of an internal error, this condition now results in a regular error message during compilation.

Simulation

- For designs that target an Arria V, Cyclone V, or Stratix V device, fixes a Synopsis® VCS® compilation error that could occur when simulating a Hard IP (HIP) for PCIe Root Port (RP) device under test (DUT) configured with the Avalon Memory-Mapped interface.

Chip Planner

- Eliminates an internal error that could occur when you open the Chip Planner or Change Manager window.

Netlist Viewers

- Eliminates an internal error that could occur in Netlist Viewers when you view a SystemVerilog design that includes a bidirectional pin.
- Fixes a problem in the Netlist Viewer that might cause the constant value of a bus signal in reverse order

PowerPlay Power Analyzer

- Fixes an internal error that might occur during power analysis of a design that targets an Cyclone V device, includes a transceiver and the transceiver uses an fPLL as a transmitter PLL.

System Console

- Fixes an error that prevented the System Console GUI from opening if the file MSVCR71.dll is not present on your computer. The error message displayed was:

```
system-console.exe - System Error
The program can't start because MSVCR71.dll is missing from your
computer. Try reinstalling the program to fix this problem.
```

Transceiver Toolkit

- Fixes a problem in the Transceiver Toolkit that caused DFE adaptation values in the combined Autosweep + EyeQ mode to be nonoptimal.
- Fixes a fatal error in the Transceiver Toolkit that might occur when you open a custom link between two boards.

DSP Builder

- Fixes a problem with the DSP Builder Standard IO&Bus::AltBus block. In previous versions of DSP Builder, the block was producing functionally incorrect HDL for signed-to-unsigned conversions when saturation was enabled.
- Fixes a problem introduced in DSP Builder Advanced Version 13.1 that affected designs that us the BusStimulusFileReader block in a subsystem that is not an ancestor to the DUT synthesized subsystem. The fix ensures that blocks that are enclosed in multiply nested subsystems are found and the appropriate test bench code is generated.
- Fixes a problem that prevented MathWorks MATLAB R2013b from simulating a design that uses the NCO ModelIP block.

IP

- IP cores released with the Altera Complete Design Suite Version 13.1 Update 2 have a version of 13.1.

EMIF IP Cores

- Allows you to mask groups and ranks from calibration in UniPHY IP in the External Memory Interface (EMIF) Debug Toolkit. To use this feature, you need to regenerate the UniPHY IP after installing update 2.
- Corrects the initialization sequence for DDR3 LRDIMMs that use components with x4 DQS widths
- Fixes a migration issue from the Quartus II software Version 13.0 SP1 DP5 to Version 13.1. When a top-level EMIF wrapper generated in version 13.0 SP1 DP5 was opened in version 13.1, the parameter editor GUI was reset to its default values. This fix maintains your design-specific parameters from version 13.0 SP1 DP5.

HSSI IP

- Fixes an issue that affected designs that targeted 5CSXFC4 and 5CSXFC2 devices in the Cyclone V family when HSSI-related input ports are tied to logic `1` or logic `0`. This update ensures that the connectivity implied by the netlist is maintained.
- For designs that target Arria II GX, Arria II GZ, Cyclone IV GX, Stratix IV GX, and Stratix IV GT devices, allows the `inclk[0]` port of a HSSI PLL to be left open. Previous versions of the Quartus II software required the `inclk[0]` port of an HSSI PLL to be driven.

PCI Express®

- For designs that target Arria V, Cyclone V, and Stratix V devices, fixes a problem that prevented the MegaWizard Plug-In Manager from automatically launching an IP variant that had been created with the PCIe Hard IP MegaWizard.
- For designs that target Arria® V devices, fixes a problem that affected the LTSSM within the PHY MAC in the Hard IP (HIP). In previous versions of the Altera Complete Design Suite, the Clock Generation Block (CGB) in the PMA does not get reset by digital reset when there is a speed switch, causing the LTSSM to loop between `Detect` and `Polling.Active` and to not proceed to `Polling.Config`, leading to a time out in Gen2 PCI Express (PCIe®) designs on Arria V ES and production devices. To apply this fix, regenerate the IP and recompile after installing update 2.
- For designs that target Arria V, Cyclone V, and Stratix V devices, fixes an issue with the PCIe MegaWizard Plug-In Manager, allowing variants to be successfully regenerated.
- Fixes an issue with the PCIe HIP when using the Avalon Memory-Mapped (Avalon-MM) interface with fixed address translation enabled. The issue affected designs that target Arria II GX, Cyclone IV GX, and Stratix IV GX devices.

VIP Suite

- Updates some false paths for the clocked video input (CVI) that are necessary for timing closure. Without the update, designs using the CVI are prone to timing failure that results in non-operational designs. Whether the design synthesized will operate has been observed as intermittent without the update. If designs using the CVI consistently function when programmed, then the observed change from this update is cleaner TimeQuest Timing Analyzer results. If multiple synthesis runs are required to generate an operational design, this update removes that inconsistency.

Issues Addressed in Update 1

The Altera Complete Design Suite Version 13.1 Update 1 (included with Update 2) addresses the following software issues:

Device Support

- Provides full compilation and programming support for the following Arria V devices: 5ASXMB3E4F31I3 and 5ASXMB5E4F31I3.
- Provides full compilation and programming support for the following Cyclone V devices: 5CSEMA2, 5CSEBA2, 5CSXFC2, 5CSEMA4, 5CSEBA4, 5CSXFC4.
- Fixes an issue in the Quartus II software Version 13.1 related to minor temperature-related routing resistance variances for Cyclone V devices and reverts timing delays to match those in the Quartus II software Version 13.0 SP1. The impact to designs compiled with version 13.1 was small and is unlikely to cause a silicon issue.

Nios II EDS

- Corrects an issue that caused some Nios II EDS utilities to fail with no error output or messages when run on a Windows PC. The affected utilities are: `sof2flash`, `elf2flash`, `elf2hex` and `bin2flash`.

Qsys

- Adds UART1 pin location information for Arria V SoCs to the Peripherals Pin Multiplexing tab in Qsys.

Quartus II Compilation Flows

- Fixes missing Arria V GZ Programmable Power Technology Optimization settings on the **More Settings** panel of the **Fitter Settings** dialog box in the Quartus II software.
- Fixes an internal error that was generated when a PLL clock is routed to external IO pin with a `create_generated_clock` SDC assignment.
- Prevents an internal error in Advanced Single Event Upset (SEU) Detection, CvP Update, and Partial Reconfiguration flows when Strictly Preserved logic is placed into a single 1x1 Logic Lock region with no preserved routes leaving or entering the region.
- Fixes an issue in the Fitter where LVDS input buffers are powered by VCCPD, but VCCIO was mistakenly assigned to LVDS input pins with differential OCT.
- Fixes a problem with the register packer where register banks could be accidentally merged within DSP inputs when the input to the Fitter came from third party synthesis tools.
- Fixes an issue in which the Quartus II Fitter fails to place one or more nodes, including at least one dual-regional clock driver, generating an Error message similar to
  `Error (175001): Could not place dual-regional clock driver`
  In previous versions of the Quartus II software, this error occurred after the Fitter indicated that it had successfully placed all clocks in the design through messages like
  `Info (11178): Promoted <x> clocks...` or
  `Info (11191): Automatically promoted <x> clocks...`
- Removes incorrect error messages that can occur when using the Engineering Change Order (ECO) Fitter flow.
- Fixes an issue with VCCIO, VCCPD, and VCCN voltage rail settings in Stratix V 5SGXMBBR2H40I2L devices. Previous versions of the Quartus II software ignored a Quartus II Settings File (.qsf) assignment of `set_global_assignment -name STRATIX_DEVICE_IO_STANDARD "1.8 V"` and the I/O banks remained at 2.5 V.

Transceiver Toolkit

- Fixes an issue in the Transceiver Toolkit that caused receiver-only autosweep to always report a bit error rate of 1.

Simulation

- In previous versions of the Quartus II software, simulation of a Stratix V example design with a VHDL testbench fails in NCSIM because:
  1. Multiple copies of same file were being generated. NCSIM is not able to bind the instance to the correct module.
  2. Port corresponding to the unused lanes were not terminated during file generation.

  In Update 1, the above mentioned issues are fixed. Regenerate the files to simulate the VHDL example design in NCSIM.
- Fixes a simulation mismatch at the outputs of an adder when performing multiple DSP chaining with 18x18+36 mode through HDL code (inferencing). In previous versions of the Quartus II software, there was a chance to have a functionality issue if the input is signed and the result width for each DSP blocks are different.
- Removes unnecessary notification messages during simulation. The removed messages are of the form:
  `Input frequency on DLL instance <name> now matches with specified clock frequency.`

DSP Builder

- Fixes DSP Builder Advanced incorrectly merging duplicate delays that have configuration differences:
  - between the status of the minimum delay checkbox
  - equivalence group, if minimum delay has been checked.
- Fixes the following issues in DSP Builder Advanced optimization of constant fixed-point sub-expressions:
  - Addition and subtraction of signals with differing fraction lengths
  - Comparing signals with 0
  - Adding and subtracting without word growth and comparing with a constant
  - Comparing signals with differing fraction lengths
  - Bitwise ANDing and ORing of signals with differing fraction length
  - Adding and subtracting of non-zero constants with non-constant signals

IP

Ethernet IP Cores

- Fixes a problem in the KR4 Configuration of the 40G/100G Ethernet Megacore where reads from the MAC RX Statistics Registers may return invalid data.
- Enables MAC 10/100 half duplex support in the 10/100Mb Small MAC variation of the Triple-Speed Ethernet IP core.

EMIF IP Cores

- Fixes the behavior of the timing counters used during the power-on memory initialization and reset period of DDR memory interfaces. In previous versions of the Quartus II software, these timers assumed an AFI clock period of 266 MHz, therefore interfaces with AFI clock frequencies faster than 266 MHz had slightly shorter reset and initialization periods than the JEDEC-required specification. This change now adjusts the counters according to the AFI frequency such that the initialization time remains constant irrespective of interface frequency or rate. This change also ensures that the `Tinit` value specified in the MegaWizard Plug-In Manager under the **Memory Timing** tab modifies the initialization counter accordingly. Previous versions of Quartus hard-coded the memory initialization time to 500 µs.
  - Device Families Affected: Arria V, Cyclone V, Stratix IV, and Stratix V
  - Protocols Affected: DDR2 and DDR3 (for AFI clock frequencies greater than 266 MHz).
- Previous versions of the Quartus II software did not properly configure the memory controller for the Hard Processor Subsystem (HPS) when an LPDDR2 memory interface is selected in Arria V SoC and Cyclone V SoC devices. This problem manifests as a calibration failure error during the memory initialization phase. This update fixes this issue and this fix is recommended for any customer using LPDDR2 on an HPS.
  - Device Families Affected: Arria V SoC and Cyclone V SoC
  - Protocols Affected: LPDDR2
- In the Altera Complete Design Suite Version 13.1, EMIF IP cores incorrectly issued a warning to indicate that Cyclone V timing models are preliminary. However, the last Cyclone V (nonSoC) timing models became final in ACDS 13.1. This update removes the EMIF IP preliminary timing model warning.

Software Issues Resolved

The following Customer Service Requests were fixed or otherwise resolved in the Altera Complete Design Suite version 13.1 Update 4:

Customer Service Request Numbers Resolved in the Altera Complete Design Suite Version 13.1 Update 4							
10985490	11007587	11008081	11012418	11019022	11024080	11027226	11029537
11030682	11034386	11030866	—	—	—	—	—

The following Customer Service Requests were fixed or otherwise resolved in the Altera Complete Design Suite version 13.1 Update 3:

Customer Service Request Numbers Resolved in the Altera Complete Design Suite Version 13.1 Update 3							
10962447	11002644	11013006	11015764	11020835	11022522	11025397	11027175

The following Customer Service Requests were fixed or otherwise resolved in the Altera Complete Design Suite version 13.1 Update 2:

Customer Service Request Numbers Resolved in the Altera Complete Design Suite Version 13.1 Update 2							
10900722	10954006	10992650	10992883	11001656	11003696	11004120	11004934
11005290	11006004	11007341	11007811	11008366	11009476	11009884	11012523
11012860	11013336	11014409	—	—	—	—	—

The following Customer Service Requests were fixed or otherwise resolved in the Altera Complete Design Suite version 13.1 Update 1:

Customer Service Request Numbers Resolved in the Altera Complete Design Suite Version 13.1 Update 1							
10862388	10865226	10957886	10990717	10995942	11001820	11002391	11004954
11005496	11007025	11007465	—	—	—	—	—

Software Patches Included

The Altera Complete Design Suite version 13.1 Update 4 includes the following patches released for previous versions of the Altera Complete Design Suite software:

Quartus II Software Version	Patch	Customer Service Request Number	Quartus II Software Version	Patch	Customer Service Request Number
13.1	0.49	11007587	13.1.2	2.02	11027226
13.1	0.69	11030866	13.1.2	2.04	11007587
13.1.1	1.04	11019022	13.1.3	3.03	11034386
13.1.1	1.07	10985490	13.1.3	3.04	11019022

Altera SDK for OpenCL Version	Patch	Customer Service Request Number	Altera SDK for OpenCL Version	Patch	Customer Service Request Number
13.1	0.02cl	11030682	—	—	—

The Altera Complete Design Suite version 13.1 Update 3 includes the following patches released for previous versions of the Altera Complete Design Suite software:

Quartus II Software Version	Patch	Customer Service Request Number	Altera SDK for OpenCL Version	Patch	Customer Service Request Number
13.1	0.39	10962447	13.1	0.01	—
13.1	0.56	11022522	—	—	—
13.1.1	1.06	11015764	—	—	—

The Altera Complete Design Suite version 13.1 Update 2 includes the following patches released for previous versions of the Altera Complete Design Suite software:

Quartus II Software Version	Patch	Customer Service Request Number	Quartus II Software Version	Patch	Customer Service Request Number
13.1	0.44	11004120	13.1	0.15	10992883
13.1	0.37	—	13.0	0.47	10992650
13.1	0.36	11012860	13.0sp1	1.dp5s	11001656
13.1	0.28	11009884	—	—	—

The Altera Complete Design Suite version 13.1 Update 1 includes the following patches released for previous versions of the Altera Complete Design Suite software:

Quartus II Software Version	Patch	Customer Service Request Number	Quartus II Software Version	Patch	Customer Service Request Number
13.1	0.24	10957886,10990717	13.1	0.04	11002391
13.1	0.20	—	13.1	0.02	10995942
13.1	0.16	10862388	13.0 SP1	1.dp5e	—
13.1	0.11	10845226	13.0 SP1	1.67	10957886
13.1	0.07	11004954	13.0 SP1	1.51	10865226
13.1	0.05	11001820	13.0	0.48	10957886

Latest Known Altera Complete Design Suite Issues

Description	Workaround
After installing the Altera Complete Design Suite Version 13.1 Update 3, you might see an error message when simulating designs targeting Arria V, Cyclone V, or Stratix V devices with Altera PLL IP with the Mentor Graphics® ModelSim-Altera® software. The error message for VHDL users is `Error: Unknown formal identifier "pll_slf_rst"`, and the error message for Verilog users is `Error: Unresolved defparam reference to "pll_slf_rst"`.	To eliminate the error, compile the following files into a local library directory, and map the altera_lnsim and altera_lmsim_ver libraries to this directory: **quartus\eda\sim_lib\altera_lnsim.sv** **quartus\eda\sim_lib\altera_lnsim_components.vhd** (VHDL only)
If you install the DSP Builder Version 13.1 after you install a Quartus II software Version 13.1 Update to your Quartus II software Version 13.1, you will encounter a version mismatch error.	To eliminate the error, perform the following tasks: 1. Uninstall the Quartus II software Version 13.1 Update. 2. Install the DSP Builder Version 13.1. 3. Reinstall the Quartus II software Version 13.1 Update.

For more information about known software issues, can find known issue information refer to the Knowledge Database page at the following URL:

http://www.altera.com/support/kdb/kdb-index.jsp

For technical support information about the Quartus II software, refer to the **Quartus II Software Support** page at the following URL:

http://www.altera.com/support/software/sof-quartus.html

Document Revision History

The following table shows the revision history for this document.

Document Revision History

Date	Version	Changes
March 2014	13.1.4.0	Added update 4 information.
February 2014	13.1.3.0	Added update 3 information.
January 2014	13.1.2.0	Added update 2 information.
December 2013	13.1.1.0	Initial release.