

This document provides late-breaking information about the Altera® Quartus® II software version 13.0 SP1.

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For information about operating system support, refer to the **readme.txt** file in your **altera/<version number>/quartus** directory. For the latest information about the MegaCore® IP Library, refer to the *MegaCore IP Library Release Notes and Errata*.

## New Features & Enhancements

The Quartus II software version 13.0 SP1 includes the following new features and enhancements:

- Enhanced device support:
  - Full device support for the following Arria<sup>®</sup> V devices: 5ASXB3, 5ASXB5, 5ASTD3, and 5ASTD5
  - Full device support for the following Cyclone<sup>®</sup> V device: 5CGXC3
  - Advance device support for the following Cyclone V device: 5CSEA2, 5CSEA4, 5CSXC2, 5CSXC4
- The Sentinel software guard driver now supports Microsoft Windows versions 7 and 8. The driver is located at **quartus/drivers/sentinel/win7/sentinst.exe** in your Quartus II software version 13.0 SP1 installation.
- Qsys now has a new reset controller for asynchronous reset of Qsys systems. This new reset controller prevents corruption of on-chip memory content after an asynchronous reset. Qsys automatically upgrades existing designs to this new reset controller.
- You can use the Quartus II Help with the following browsers:
  - Local Quartus II Help is fully compatible with Mozilla Firefox 3.6 running on Linux 32-bit systems.
  - Quartus II Web Help (hosted at <http://quartushelp.altera.com/current>) is fully compatible with Google Chrome, Safari 5, Microsoft Internet Explorer 9, and Mozilla Firefox 20.0.
  - Some Help features require that you to disable pop-up blocking.

## Memory Recommendations

A full installation of the Quartus II software requires up to 18 GB of available disk space on the drive or partition where you are installing the Altera software.

The Quartus II Stand-Alone Programmer requires a minimum of 1 GB of RAM plus additional memory, based on the size and number of SRAM Object Files (.sof) files and the size and number of devices being configured.

Altera recommends that your system be configured to provide virtual memory equal to the recommended physical RAM that is required to process your design.

The following table lists the memory required to process designs targeted for Altera devices.

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
Arria GX	EP1AGX20	512 MB	512 MB
	EP1AGX35, EP1AGX50, EP1AGX60	1.0 GB	1.5 GB
	EP1AGX90	1.5 GB	2.0 GB
Arria II GX	EP2AGX45	1.0 GB	1.5 GB
	EP2AGX65	1.5 GB	2.0 GB
	EP2AGX95, EP2AGX125, EP2AGX190	3.0 GB	4.0 GB
	EP2AGX260	4.0 GB	6.0 GB
Arria II GZ	EP2AGZ225	3.0 GB	4.0 GB
	EP2AGZ300	4.0 GB	6.0 GB
	EP2AGZ350	Not recommended	8.0 GB
Arria V	5AGXA1	Not recommended	6.0 GB
	5AGTC3, 5AGXA3, 5AGXA5	Not recommended	8.0 GB
	5AGXA7, 5AGTC7	Not recommended	10.0 GB
	5AGXB1, 5AGXB3, 5AGTD3, 5ASTD3, 5ASXB3	Not recommended	12.0 GB
	5AGXB5, 5AGTD7, 5AGXB7, 5ASXB5, 5ASTD5	Not recommended	16.0 GB
Arria V GZ	5AGZE1	Not recommended	8.0 GB
	5AGZE3, 5AGZE5	Not recommended	12.0 GB
	5AGZE7	Not recommended	16.0 GB
Cyclone	All	512 MB	512 MB
Cyclone II	EP2C5, EP2C8, EP2C15, EP2C20	512 MB	512 MB
	EP2C35, EP2C50	1.0 GB	1.5 GB
	EP2C70	1.5 GB	2.0 GB
Cyclone III	EP3C5, EP3C10, EP3C16, EP3C25, EP3C40	512 MB	512 MB
	EP3C55, EP3C80	768 MB	1.0 GB
	EP3C120	1.5 GB	2.0 GB
Cyclone III LS	EP3CLS70, EP3CLS100	1.5 GB	2.0 GB
	EP3CLS150, EP3CLS200	3.0 GB	4.0 GB

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
Cyclone IV E	EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, EP4CE40	512 MB	512 MB
	EP4CE55, EP4CE75	768 MB	1.0 GB
	EP4CE115	1.0 GB	1.5 GB
Cyclone IV GX	EP4CGX15, EP4CGX22, EP4CGX30	512 MB	512 MB
	EP4CGX50, EP4CGX75	1.0 GB	1.5 GB
	EP4CGX110, EP4CGX150	1.5 GB	2.0 GB
Cyclone V	5CEA2, 5CGXC3, 5CEA4, 5CGXC4, 5CEA5, 5CGTD5, 5CGXC5, 5CSEA5, 5CSTD5, 5CSXC5, 5CSEA6, 5CSXC6, 5CEA7, 5CGTD7, 5CGXC7, 5CSEA2, 5CSEA4, 5CSXC2, 5CSXC4, 5CSTD6	Not recommended	6.0 GB
	5CEA9, 5CGTD9, 5CGXC9	Not recommended	8.0 GB
HardCopy® II	HC210, HC210W	1.5 GB	2.0 GB
	HC220, HC230, HC240	3.0 GB	4.0 GB
HardCopy III	HC325	Not recommended	8.0 GB
	HC335		12.0 GB
HardCopy IV	HC4E25	Not recommended	8.0 GB
	HC4GX15		12.0 GB
	HC4E35, HC4GX25		16.0 GB
	HC4GX35		20.0 GB
MAX®	All	512 MB	512 MB
MAX II	All	512 MB	512 MB
MAX V	All	512 MB	512 MB
Stratix	EP1S10, EP1S20	512 MB	512 MB
	EP1S25, EP1S30, EP1S40, EP1S60	1.0 GB	1.5 GB
	EP1S80	1.5 GB	2.0 GB
Stratix GX	EP1SGX10	512 MB	512 MB
	EP1SGX25, EP1SGX40	1.0 GB	1.5 GB
Stratix II	EP2S15	512 MB	512 MB
	EP2S30	1.0 GB	1.5 GB
	EP2S60, EP2S90	1.5 GB	2.0 GB
	EP2S130, EP2S180	3.0 GB	4.0 GB
Stratix II GX	EP2SGX30, EP2SGX60	1.0 GB	1.5 GB
	EP2SGX90	1.5 GB	2.0 GB
	EP2SGX130	3.0 GB	4.0 GB
Stratix III	EP3SL50, EP3SE50, EP3SL70	1.0 GB	1.5 GB
	EP3SE80	1.5 GB	2.0 GB
	EP3SL110, EP3SE110, EP3SL150, EP3SL200	3.0 GB	4.0 GB
	EP3SE260, EP3SL340	4.0 GB	6.0 GB

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
Stratix IV	EP4SGX70	1.5 GB	2.0 GB
	EP4SE230 EP4SGX110, EP4SGX230, EP4S40G2, EP4S100G2	3.0 GB	4.0 GB
	EP4SGX290	4.0 GB	6.0 GB
	EP4SE360 EP4SGX360, EP4S100G3, EP4S100G4	Not recommended	8.0 GB
	EP4SGX530, EP4SE530, EP4SE820, EP4S40G5, EP4S100G5	Not recommended	12.0 GB
Stratix V	5SGSD3	Not recommended	8.0 GB
	5SGXA3, 5SGSD4, 5SGXA4, 5SGTC5	Not recommended	12.0 GB
	5SGSD5, 5SGXA5, 5SGXB5, 5SGSD6, 5SGXB6	Not recommended	16.0 GB
	5SGTC7, 5SGXA7, 5SGSD8	Not recommended	20.0 GB
	5SGXA9, 5SEE9	Not recommended	24.0 GB
	5SEEB, 5SGXAB, 5SGXB9, 5SGXBB	Not recommended	28.0 GB

## Changes in Device Support

The following section is divided into device support changes according to whether the change is a notification, and whether the change has been fixed or not fixed.

Description	Workaround
<b>Change Notifications</b>	
<b>Device Support Not Fixed</b>	
<p><b>USB Blaster II device drivers not automatically installed</b></p> <p>The USB-Blaster™ II device drivers require manual installation so that the cable will be properly recognized.</p>	<ol style="list-style-type: none"> <li>1. Plug in the USB-Blaster II.</li> <li>2. Open the <b>Device Manager</b> and right-click on the <b>Unknown device</b> under the <b>Other devices</b> branch.</li> <li>3. Select <b>Update Driver Software</b>.</li> <li>4. Select <b>Browse my computer for driver software</b>.</li> <li>5. Enter the location of the Quartus II software USB-Blaster II driver files directory (&lt;quartus&gt;/drivers/usb-blaster-ii) in the <b>Search for driver software in this location</b> field.</li> <li>6. Click <b>Next</b>.</li> <li>7. Click <b>Install</b> in the <b>Would you like to install this device software?</b> Windows security dialog box.</li> <li>8. Close the <b>Update Driver Software - Altera USB-Blaster II (Unconfigured)</b> successful installation notification. The Device Manager now shows a new branch called <b>JTAG cables</b> with an <b>Altera USB-Blaster II (Unconfigured)</b> node.</li> <li>9. Open the Quartus II Programmer. Within a few seconds, the <b>JTAG cables</b> branch displays two nodes: <b>Altera USB-Blaster II (JTAG interface)</b> and <b>Altera USB-Blaster II (System Console interface)</b>.</li> </ol>
<p><b>Incorrect synthesis when top-level VHDL entity has unconstrained ports</b></p> <p>The netlist cannot be generated when ports of variable dimensions are defined in the top-level VHDL entity.</p>	<p>Declare the dimensions of all ports in the top-level VHDL entity before netlist generation.</p>
<p><b>Assign LVDS I/O standard-supported pins in right I/O banks of Arria V A1/A3/C3 devices as PLL clock input pins only</b></p> <p>If you use the Quartus II software version 13.0 DP2 or 13.0 SP1 to create a design that targets an Arria V A1, A3, or C3 device, and you use the LVDS I/O standard-enabled pins in the right I/O bank for purposes other than as phase-locked loop (PLL) clock input pins, the resulting FPGA hardware might not function properly.</p>	<p>You must assign the LVDS I/O standard-enabled pins in the right I/O bank as PLL clock input pins only. The Quartus II software version 13.0 DP2 or 13.0 SP1 does not issue an error message for incorrect assignments to these LVDS I/O standard-enabled pins.</p>

Description	Workaround
<p><b>Error issued when importing database that uses the DPA feature prior to 13.0 SP1</b></p> <p>A design compiled in a Quartus II software version earlier than 13.0 SP1 that targets an Arria V, Arria V GZ, or Stratix V device and that uses the DPA feature encounters an error when its database is imported into the Quartus II software version 13.0 SP1 or later.</p>	<p>Recompile the design to generate a valid programming file.</p>
<p><b>The Quartus II software does not automatically detect and update IP cores for PCIe®</b></p> <p>When creating a design with an IP core for PCI Express® (PCIe) in Qsys prior to version 12.1, <b>Regenerate IP Component</b> in the Quartus II software does not automatically update the PCIe IP core to the current version.</p>	<p>To avoid compilation errors, regenerate your Qsys system manually prior to compilation. To regenerate the Qsys system:</p> <ol style="list-style-type: none"> <li>1. In the Quartus II software, open your project.</li> <li>2. Click <b>Tools &gt; Qsys</b> to open Qsys.</li> <li>3. Open the Qsys system that includes the PCIe IP core.</li> <li>4. Click the <b>Generation</b> tab.</li> <li>5. Click <b>Generate</b>.</li> </ol>
<p><b>Upgrade IP Components dialog box does not recognize some IP changes from version 13.0 to 13.0 SP1</b></p> <p>The Upgrade IP Components feature in the Quartus II software version 13.0 SP1 does not recognize some optional IP updates between versions 13.0 and 13.0 SP1. Affected IP cores are known to include the following MegaCore functions:</p> <ul style="list-style-type: none"> <li>■ CPRI</li> <li>■ DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP</li> <li>■ DDR3 SDRAM Controller with ALTMEMPHY</li> <li>■ DDR2, DDR3, and LPDDR2 SDRAM Controller with UniPHY</li> <li>■ FFT</li> <li>■ SDI</li> <li>■ SDI II</li> <li>■ Triple Speed Ethernet</li> <li>■ Video and Image Processing Suite</li> </ul>	<p>For information about updates made to an IP core in version 13.0 SP1, consult the chapter pertaining to that IP core in the <a href="#">MegaCore IP Library Release Notes and Errata</a> version 13.0 SP1.</p>
<p><b>Error: Voltage Value 1.2V is not supported by part</b></p> <p>In the Quartus II software version 13.0 SP1, if a design:</p> <ul style="list-style-type: none"> <li>■ targets an Arria V GX device, and</li> <li>■ VCCR_GXB is set to 1.2 V, or</li> <li>■ VCCT_GXB is set to 1.2 V</li> </ul> <p>compilation fails with an error similar to the following:</p> <pre>Internal Error: Sub-system: CUT, File: /quartus/db/cut/cut_stratixv_hssi_pma_util.cpp, Line: 1434 Voltage Value 1.2V is not supported by part</pre>	<p>Change the following assignment in your Quartus II Settings File (.qsf)</p> <pre>set_instance_assignment -name XCVR_VCCR_VCCT_VOLTAGE 1_2V -to &lt;PIN&gt; to set_instance_assignment -name XCVR_VCCR_VCCT_VOLTAGE 1_15V -to &lt;PIN&gt; or set_instance_assignment -name XCVR_VCCR_VCCT_VOLTAGE 1_1V -to &lt;PIN&gt;</pre>

Description	Workaround
<p><b>Recommended VCCR_GXB and VCCT_GXB settings for Arria V GX C6 designs that run transceivers at less than or equal to 3.125 Gbps</b></p> <p>If your design targets an Arria V GX C6 device and implements a data rate less than or equal to 3.125 Gbps, Altera recommends setting VCCR_GXB and VCCT_GXB to 1.1 V to reduce power consumption. The Quartus II software sets the default VCCR_GXB and VCCT_GXB settings to 1.15 V. You may change the VCCR_GXB and VCCT_GXB settings to 1.1 V manually.</p>	<p>Add the following assignment to your Quartus II Settings File (.qsf):</p> <pre>set_instance_assignment -name XCVR_VCCR_VCCT_VOLTAGE 1_1V -to *</pre>
<b>Device Support Fixed</b>	
<p><b>Some IBIS models contain incorrect timing parameters</b></p> <p>Some IBIS models are found to have incorrect values for the following IBIS timing parameters:</p> <p>Vmeas, Rref, Rref_diff, Vref, Vinh and Vinl</p>	<p>This issue is corrected in the Quartus II software version 13.0.</p>
<p><b>Arria V GX VCCR_GXBR and VCCT_GXB power rail voltage change</b></p> <p>Pin-out and power reports in the Quartus II software version 13.0 incorrectly reported Arria V GX VCCR_GXB and VCCT_GXB voltage as 1.2 V. The correct voltage is 1.15 V.</p>	<p>This issue is corrected in the Quartus II software version 13.0 SP1.</p>
<p><b>Arria V ST VCCR_GXBR and VCCT_GXB power rail voltage change</b></p> <p>Pin-out and power reports in the Quartus II software version 13.0 incorrectly reported Arria V GT VCCR_GXB and VCCT_GXB voltage as 1.15 V. The correct voltage is 1.2 V.</p>	<p>This issue is corrected in the Quartus II software version 13.0 SP1.</p>
<p><b>Arria V timing models changed in the Quartus II software version 13.0</b></p> <p>Arria V timing models have changed. Some of these changes affect devices which had been at "Final" timing status.</p>	<p>Updates were made to the final timing models in version 13.0. Refer to solution number <a href="#">rd04252013_701</a> in the Altera Knowledge Base.</p>
<p><b>Stratix V timing model changed in the Quartus II software version 13.0 : clr input of M20K blocks</b></p> <p>The clr input of M20K memories, when driven directly by a global, regional, or periphery clock buffer is not analyzed by the TimeQuest timing analyzer in the Quartus II software version 12.1 SP1 and earlier. This change affects devices that had been at "Final" timing status.</p>	<p>Updates were made to the final timing models in version 13.0. Refer to solution number <a href="#">rd02202013_401</a> in the Altera Knowledge Base.</p>
<p><b>Stratix V timing model changed in the Quartus II software version 13.0: Logic and routing delays</b></p> <p>A software error in the Quartus II software version 12.1 SP1 and earlier caused minor timing modeling errors for some logic and routing delays (typically &lt; 20 ps). This change affects devices that had been at "Final" timing status.</p>	<p>Updates were made to the final timing models in version 13.0. Refer to solution number <a href="#">rd02202013_401</a> in the Altera Knowledge Base.</p>
<p><b>VCCRSTCLK_HPS pin labelled incorrectly</b></p> <p>The VCCRSTCLK_HPS pin was incorrectly labelled as "VCC_HPS." Applies to some Cyclone V SoC devices.</p>	<p>Refer to the updated pinout table to identify both VCCRSTCLK_HPS pins.</p>



Description	Workaround
<p><b>Ordering Part Number (OPN) change for Cyclone V E50 devices.</b></p> <p>Some OPNs have been identified as incorrect.</p>	<p>5CEFA2 devices become 5CEBA2 devices</p> <p>5CEFA4 devices become 5CEBA4 devices</p>
<p><b>No pipe_pclk output issue</b></p> <p>The pipe_pclk clock cannot be activated on a non-global clock.</p>	<p>The pipe_pclk clock must be on a global clock signal to function properly.</p>
<p><b>CPRI placement on restricted triplet issue</b></p> <p>Previous restrictions on Ch0, Ch1, and Ch2 in GXB_L0 and GXB_R0 is updated in the Quartus II software 12.1. Ch0 in both GXB_L0 and GXB_R0 is now available for deterministic latency protocols.</p> <p>Applies to Arria V devices</p>	<p>—</p>

## Changes to Software Behavior

This section documents instances in which the behavior and default settings of the Quartus II software have been changed from earlier releases of the software.

Refer to the Quartus II Default Settings File (.qdf), `<Quartus II installation directory>/quartus/bin/assignment_defaults.qdf`, for a list of all the default assignment settings for the latest version of the Quartus II software.

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
<p><b>Rapid Recompile feature not available</b></p> <p>The Rapid Recompile feature is disabled in this release.</p>	<p>There is no workaround.</p>
<p><b>Upcoming changes to .svd file generation in Qsys</b></p> <p>For designs that use .svd files in conjunction with the Hard Processor System (HPS) of SoC devices, Qsys in the Quartus II software version 13.0 SP1 generates duplicate .svd files in both the <code>&lt;project_name&gt;</code> directory and the <code>&lt;project_name&gt;/synthesis</code> directory.</p> <p>Future versions of Qsys will no longer generate .svd files in the <code>&lt;project_name&gt;</code> directory.</p> <p>If you instantiate the HPS as part of a custom <code>_hw.tcl</code> composed component, Qsys in the Quartus II software version 13.0 SP1 generates two identical .svd files:</p> <ul style="list-style-type: none"> <li>■ <code>&lt;project&gt;_&lt;submodule&gt;_&lt;interface_or_address_group_name&gt;.svd</code></li> <li>■ <code>&lt;project&gt;_&lt;submodule&gt;_&lt;submodule_in_composition&gt;_&lt;interface_or_address_group_name&gt;.svd</code></li> </ul> <p>Future versions of Qsys will no longer generate the <code>&lt;project&gt;_&lt;submodule&gt;_&lt;interface_or_address_group_name&gt;.svd</code> file.</p>	<p>Do not use the files generated in the <code>&lt;project_name&gt;</code> directory. Use the files generated in the <code>&lt;project_name&gt;/synthesis</code> directory instead.</p> <p>Do not use the <code>&lt;project&gt;_&lt;submodule&gt;_&lt;interface_or_address_group_name&gt;.svd</code> file. Use the <code>&lt;project&gt;_&lt;submodule&gt;_&lt;submodule_in_composition&gt;_&lt;interface_or_address_group_name&gt;.svd</code> file instead.</p>

## Device Support and Pin-Out Status

This section contains information about the device support status in the Quartus II software version 13.0 SP1.

### Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the new devices listed in the following table.

Device Family	Devices	
Arria V	5AGXA1	5AGXA3
	5AGXA5	5AGXA7
	5AGXB1	5AGXB3
	5AGXB5	5AGXB7
	5AGTC3	5AGTC7
	5AGTD3	5AGTD7
	5ASXB3	5ASXB5
	5ASTD3	5ASTD5
Arria V GZ	5AGZE1	5AGZE3
	5AGZE5	5AGZE7
Cyclone V	5CEA2	5CEA4
	5CEA5	5CEA7
	5CEA9	5CGXC3
	5CGXC4	5CGXC5
	5CGXC7	5CGXC9
	5CGTD5	5CGTD7
	5CGTD9	5CGXC7ES
	5CEA7ES	5CSEA6ES
	5CSXC6ES	—
Stratix V	5SEE9	5SEEB
	5SGXA9	5SGXAB
	5SGXB5	5SGXB6
	5SGXB9	5SGXBB
	5SGSD6	5SGSD8

## Advance Device Support

Compilation, simulation, and timing analysis support is provided for the devices listed in [Table 1](#) that will be released in the near future. The Compiler generates pin-out information for these devices in this release, but does not generate programming files.

**Table 1. Devices with Advance Support**

Device Family	Devices	
Cyclone V	5CSEA5	5CSEA6
	5CSXC5	5CSXC6
	5CSTD5	5CSTD6

## Initial Information Device Support

Compilation, simulation, and timing analysis support is provided for the devices listed in [Table 2](#) that will be released in upcoming versions of the Quartus II software. Programming files and pin-out information are not generated for these devices in this release.

**Table 2. Devices with Initial Information Support**

Device Family	Devices	
Cyclone V	5CSEA2	5CSEA4
	5CSXC2	5CSXC4

## Timing and Power Models

[Table 3](#) lists a summary of timing and power model status in the current version of the Quartus II software.

**Table 3. Devices with Timing and Power Models**

Device Family	Device	Timing Model Status	Power Model Status
Arria II GX	All	Correlated – 10.0 SP1	Final – 10.0
Arria II GZ	All	Final – 10.1	Final – 10.1

**Table 3. Devices with Timing and Power Models (Continued)**

Device Family	Device	Timing Model Status	Power Model Status
Arria V	5AGXB5	Final – 12.1 SP1 (3)	Preliminary
	5AGXB7	Final – 12.1 SP1 (3)	Preliminary
	5AGTD7	Final – 12.1 SP1 (3)	Preliminary
	5AGXA1	Final – 13.0 SP1	Preliminary
	5AGXA3		Preliminary
	5AGXA5	Preliminary	Preliminary
	5AGXA7	Preliminary	Preliminary
	5AGXB1	Final 13.0	Preliminary
	5AGXB3	Final 13.0	Preliminary
	5AGTC3	Final – 13.0 SP1	Preliminary
	5AGTC7	Preliminary	Preliminary
	5AGTD3	Final 13.0	Preliminary
Arria V GZ	All	Final – 12.1 SP1 (3)	Final 13.0
Arria V SoC	5ASXB3	Preliminary	Preliminary
	5ASXB5		
	5ASTD3		
	5ASTD5		
Cyclone III LS	All	Final – 10.0	Final – 10.0 SP1
Cyclone IV E	All	Final – 10.0 SP1	Final – 10.0 SP1
Cyclone IV GX	EP4CGX15	Final – 10.1	Final – 11.0
	EP4CGX22	Final – 11.0	
	EP4CGX30		Final – 11.0
	EP4CGX50	Final – 11.0	Final –11.1
	EP4CGX75		
	EP4CGX110	Final – 10.1	Final – 11.0
	EP4CGX150		
Cyclone V	5CEA2	Final – 13.0 SP1	Preliminary
	5CEA4		
	5CEA7		
	5CEA9		
	5CGXC7		
	5CGXC9		
	5CGTD7		
	5CGTD9		
	5CEA5	Preliminary	
	5CGXC3		
	5CGXC4		
	5CGXC5		
	5CGTD5		

**Table 3. Devices with Timing and Power Models (Continued)**

Device Family	Device	Timing Model Status	Power Model Status
Cyclone V SoC	5CSEA2	Preliminary	Preliminary
	5CSEA4		
	5CSEA5		
	5CSEA6		
	5CSXC2		
	5CSXC4		
	5CSXC5		
	5CSXC6		
	5CSTD5		
	5CSTD6		
HardCopy III	All	Correlated – 11.1	Correlated – 12.0
HardCopy IV E	All	Correlated – 11.1	Correlated – 12.0
HardCopy IV GX	All	Correlated – 11.1	Correlated – 12.0
MAX V	All	Final – 11.0	Final – 11.0
Stratix IV	All	Correlated – 10.0 SP1 (2)	Final – 10.1
Stratix V	5SGXA7, 5SGXA5, 5SGTC5, 5SGTC7	Final – 12.1 (3)	Final 13.0
	5SGSD3, 5SGSD4, 5SGSD5, 5SGXA3, 5SGXA4, 5SGXB5, 5SGXB6, 5SGXAB, 5SGXA9, 5SEE9, 5SEEB, 5SGXB9, 5SGXBB	Final – 12.1 SP1 (3)	Final 13.0
	5SGSD6, 5SGSD8	Final – 13.0 SP1	Final 13.0
<b>Notes to Table 3:</b>			
(1) EP4CGX30BF14 and EP4CGX30CF19 are final in 11.0, EP4CGX30CF23 final in 11.1.			
(2) The timing model is updated for PMA Direct transceiver timing in Quartus II software release 12.0.			
(3) The timing model is updated in Quartus II software version 13.0. Refer to the Device Support Fixed section for details.			

The current version of the Quartus II software also includes final timing and power models for the Arria GX, Arria II GX, Cyclone, Cyclone II, Cyclone III, Cyclone III LS, Cyclone IV E, HardCopy II, MAX, MAX II, MAX IIZ, Stratix, Stratix GX, Stratix II, Stratix II GX, Stratix III, and Stratix IV device families. Timing models for these device families became final in the Quartus II software versions 10.1 or earlier.

## IBIS Models

Table 4 lists a summary of IBIS model status in the current version of the Quartus II software.

**Table 4. Devices with IBIS Models**

<b>Device Family</b>	<b>IBIS Model Status</b>
Arria II GX	Correlated with PHY device operation – 10.0
Arria II GZ	Correlated with PHY device operation – 10.1
Arria V	Preliminary – 12.0
Cyclone III LS	Correlated with PHY device operation – 10.0
Cyclone IV E	Correlated with PHY device operation – 10.0 SP1
Cyclone IV GX	Correlated with PHY device operation – 11.0
Cyclone V	Preliminary – 12.0 SP1
HardCopy III	Preliminary – 10.0
HardCopy IV	Preliminary – 10.0
MAX V	Correlated with PHY device operation – 11.0
Stratix III	Correlated with PHY device operation – 9.1
Stratix IV	Correlated with PHY device operation – 9.1
Stratix V	Correlated with PHY device operation – 13.0 SP1

## EDA Interface Information

The Quartus II software version 13.0 SP1 supports the following EDA tools.

<b>Synthesis Tools</b>	<b>Version</b>	<b>NativeLink Support</b>
Mentor Graphics Precision RTL Synthesis	2013a	✓
Synopsys Synplify, Synplify Pro, and Synplify Premier	E-2013.03-SP1	✓
<b>Simulation Tools</b>	<b>Version</b>	<b>NativeLink Support</b>
Aldec Active-HDL	9.2 (Windows only)	✓
Aldec Riviera-PRO	2012.10	✓
Cadence INCISIV Enterprise Simulator	12.10.013 (Linux only)	✓
Mentor Graphics ModelSim®	10.1d	✓
Mentor Graphics ModelSim-Altera	10.1d	✓
Mentor Graphics Questa®	10.1d	✓
Synopsys VCS and VCS MX	2012.09-3	✓
<b>Formal Verification Tools (Equivalence Checking)</b>	<b>Version</b>	<b>NativeLink Support</b>
Cadence Encounter Conformal	8.1	—



## Antivirus Verification

The Altera Complete Design Suite version 13.0 SP1 has been verified virus free using the following software:

AVG Version: 2013.0.3272

Virus database version: 3162/1

LinkScanner version: 1591

McAfee VirusScan Enterprise + AntiSpyware Enterprise Version: 8.8

Scan Engine Version: 5400.1158

DAT Version: 7042.0000

## Software Issues Resolved

The following Customer Service Requests were fixed or otherwise resolved in the Quartus II software version 13.0 SP1:

Customer Service Request Numbers Resolved in the Quartus II Software Version 13.0 SP1							
10842787	10846159	10865226	10874308	10883672	10884631	10893162	10896142
10897606	10906463	10907345	10913650	10915236	10916129	10919100	10919765
10919897	10920889	10921445	10922385	10923187	10923665	10923668	10924140
10925342	10925386	10926230	10926256	10926540	10927161	10927737	10928261
10928696	10929079	10929308	10929797	10929807	10929864	10929934	10930031
10930507	10930511	10930576	10930706	10931630	10931662	10931983	10932500
10932748	10932786	10932792	10932812	10932865	10933084	10933249	10933700
10933723	10933915	10934334	10934365	10934493	10934516	10934581	10934722
10935046	10935121	10935374	10935693	10935965	10936157	10936161	10936171
10936224	10936788	10937002	10937118	10937318	10937711	10938059	10938497
10938539	10938865	10939262	10939380	10939459	10939595	10939653	10939677
10939897	10940032	10940168	10940288	10940373	10940406	10940407	10940631
10940704	10940729	10941070	10941214	10941511	10941785	10941891	10941910
10942285	10942372	10942536	10942618	10942808	10942828	10943023	10943390
10943501	10943782	10944059	10944151	10944179	10944227	10944360	10944533
10945046	10945059	10945191	10945378	10945500	10945506	10945587	10945889
10945936	10946017	10946593	10946665	10946666	10946674	10947026	10947044
10947070	10947178	10947190	10947214	10947241	10947536	10947603	10947890
10947974	10949360	10949362	10949467	10949469	10950047	10950127	10950315
10950340	10951193	10951196	10951246	10951566	10951667	10951749	10951803
10951857	10952012	10952256	10952328	10952555	10952573	10952615	10952832

Customer Service Request Numbers Resolved in the Quartus II Software Version 13.0 SP1							
10953501	10953931	10954013	10954172	10954311	10954694	10955081	10955152
10955171	10955245	10955586	10958025	10958351	10855815	10920143	10917015
10859939	10905673	10919327	10866105	10923237	10901541	10901548	10911201
10917496	10926845	10937371	10928420	10935131	10932326	10949909	10951500
10947317	10855046	10868828	10922848	10929559	10937392	10941936	10949093
10952736	10959971	—	—	—	—	—	—

## Software Patches Included in this Release

The Quartus II software version 13.0 SP1 includes the following patches released for previous versions of the Quartus II software:

Quartus II Software Version	Patch	Customer Service Request Number	Quartus II Software Version	Patch	Customer Service Request Number
13.0	0.28	10953364	12.1sp1	1.dp6a	—
13.0	0.22	10952000	12.1sp1	1.dp5a	—
13.0	0.18	—	12.1sp1	1.60	10941323
13.0	0.17	10934581	12.1sp1	1.55	10934179
13.0	0.14	10951193	12.1sp1	1.53	10940704
13.0	0.05	10947536	12.1sp1	1.52	—
13.0	0.03	—	12.1sp1	1.51	—
13.0	0.01	10923845	12.1sp1	1.47	10921445
12.1sp1	1.dp7j	10953932	12.1sp1	1.44	10939897
12.1sp1	1.dp7c	10950315	12.1sp1	1.34	10934334
12.1sp1	1.dp6p	10950315	12.1sp1	1.30	10930576
12.1sp1	1.dp6n	10946402	12.1	0.40	10908723
12.1sp1	1.dp6m	10936329	12.1	0.39	10936047
12.1sp1	1.dp6c	10926845	—	—	—

## Latest Known Quartus II Software Issues

For more information about known software issues, look for information on the **Quartus II Software Support** page at the following URL:

<http://www.altera.com/support/software/sof-quartus.html>

You can find known issue information for previous versions of the Quartus II software on the Knowledge Database page at the following URL:

<http://www.altera.com/support/kdb/kdb-index.jsp>

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## Document Revision History

The following table shows the revision history for this document.

### Document Revision History

Date	Version	Changes
June 2013	13.0SP1.0	Initial release