Intel® FPGA SDK for OpenCL™ Pro Edition

Version 21.1 Release Notes

Updated for Intel® Quartus® Prime Design Suite: **21.1**

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1. Intel® FPGA SDK for OpenCL™ Pro Edition Version 21.1 Release Notes

The *Intel® FPGA SDK for OpenCL™ Pro Edition Release Notes* provides late-breaking information about the Intel FPGA Software Development Kit (SDK) for OpenCL[1][2] Pro Edition and the Intel FPGA Runtime Environment (RTE) for OpenCL Pro Edition Version 21.1.

1.1. New Features and Enhancements

The Intel FPGA SDK for OpenCL Pro Edition and the Intel FPGA RTE for OpenCL Pro Edition include the following new features:

- Added the `-auto-pipeline` `aoc` command option for pipelining loops in non-task (NDRange) kernels.
- Made the following enhancements in the `report.html` file:
  - Enhanced the Loop Analysis report with a pane (Bottlenecks viewer) that shows information about loop bottlenecks.
  - Enhanced the System Viewer (*formerly known as the Graph Viewer*) to include the global memory view of the system.
  - Enhanced the Schedule Viewer report to include dependency lines that show the order of execution for the blocks and instructions in your design.
  - Enhanced the messages about the implementation of private memory in the Area Analysis of System report.

1.2. Operating System Support

Information about OS support for the Intel FPGA SDK for OpenCL is available on the Operating System Support page of the Intel FPGA website.

Related Information

Operating System Support

(1) OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission of the Khronos Group™.

(2) The Intel FPGA SDK for OpenCL is based on a published Khronos Specification, and has passed the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.

1.3. Changes to Software Behavior

Items listed in the following table represent cases in which the behaviors of the current release of the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL differ from the previous version.

- In the `math.h` header file, changed the return type of `signbit(double)` to `int`.
- Deprecated the cluster-control attribute `__attribute__((stall_enable))` and renamed it as `use_stall_enable_clusters`.
- Renamed the Graph Viewer report name as System Viewer.
- The `-ffp-reassoc` flag is not supported. Use the `fp reassociate` pragma.

Related Information

OpenCL 2.0 Headers

1.4. Known Issues and Workarounds

This section provides information about known issues that affect the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 21.1.

Description	Workaround
Full Intel Quartus® Prime compilation fails on the Intel FPGA SDK for OpenCL version 21.1 build 173.3. You might observe one of the following device-specific error messages: • When compiling the kernel using the flat flow: — **Intel Arria® 10**: `Error: Unknown device part 10AX115S2F45I1SG` — **Intel Stratix® 10**: `Error: Unknown device part 1SG280LU2F50E2VG` • When compiling the kernel using the import flow: — **Intel Arria 10**: `Error: kernel_mem_mm_bridge_0: deviceFamily "Arria 10" is out of range: "Cyclone 10 GX", "None", "Unknown"` — **Intel Stratix 10**: `Error (XXXXX): Cannot generate Atom Netlist File because family Stratix 10 is not installed`	Install the appropriate Intel Quartus Prime Pro Edition software version 21.1 Patch 0.14cl from the following links: • Windows (`.exe`) • Linux (`.run`) For additional information about the patch, refer to the `opencl-21.1-0.14cl-readme.txt` file.

When using the Intel FPGA SDK for OpenCL simulation flow, you may encounter some messages upon the exit of the host program, as shown in the following:
`mmd fatal: src/acl_msim.cpp:59: can't find handle 3`
`-- aborting`
`src/acl_msim.cpp:59: acl_msim_device* {anonymous}::get_msim_device(int): assertion `0' failed.`
	You can safely ignore these messages. The messages get displayed as a result of the simulator process not shutting down cleanly.

When compiling an OpenCL kernel containing calls to library functions containing HLS tasks, incremental compile may trigger recompilation for unaffected kernels.	No known workaround. However, this is not a functional bug. It may result in a more conservative incremental compile.
The emulator runtime emits an assertion error if a kernel is enqueued 16,000 times.	Do not enqueue a kernel more than 16,000 times.

continued...

Description	Workaround
OpenCL kernels with names longer than 61 characters might fail in the Intel Quartus Prime Pro Edition compiler with an error similar to the following error: `Error (16045): Instance "...|<long_kernel_name>_cra_slave_inst" instantiates undefined entity "<long_kernel_name>_function_cra_slave" File: <filename> Line: <linenumber>`	Reduce the size of the OpenCL kernel name.
OpenCL kernel pipes cannot be passed as arguments in some cases. The symptom is the runtime receives a `CL_INVALID_BUFFER_SIZE (-61)` error when you enqueue your kernel.	Modify your design to use channels instead of pipes.
When alternatively using sub-buffers and their parent buffers, changes written to one might not be reflected in the other.	Unmapping and mapping a buffer forces the sub-buffers and their parent buffers to be synced. Unmapping and mapping a buffer between buffer uses should prevent this issue.

This section provides information about known issues that affect the current release of the Intel FPGA SDK for OpenCL Custom Platform Toolkit and Reference Platforms. These issues might also affect Custom Platforms you create for use with the Intel FPGA SDK for OpenCL.

Description	Workaround
For Windows, when the host application queries the number of devices, calls to `clGetDeviceIDs` return 128 devices regardless of the actual number of devices present. *Note:* You can find the actual available devices at the beginning of the device list returned by `clGetDeviceIDs`.	Perform one of the following workarounds: • Rewrite the host application to limit the query for `clGetDeviceIDs` to the actual number of devices. • Rewrite the host application to use `clGetDeviceInfo` to query which devices are available. Calling `clGetDeviceInfo` with the `CL_DEVICE_AVAILABLE` flag correctly reports that extraneous devices are unavailable. • Rewrite the host application to only call `clCreateContext` with the actual number of devices. Calling `clCreateContext` with extraneous devices fails with the error `CL_DEVICE_NOT_AVAILABLE`. • Set the environment variable *`CL_OVERRIDE_NUM_DEVICES_INTELFPGA`* to the correct number of devices. Doing so fixes the erroneous behavior of `clGetDeviceIDs`.

Latest Known Intel FPGA SDK for OpenCL Software Issues

For additional known issue information for the current Intel FPGA SDK for OpenCL version and for previous versions, refer to the Knowledge Base web page.

Related Information

Knowledge Base

1.5. Software Issues Resolved

The following issues were corrected or otherwise resolved in the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 21.1.

Table 1. Issues Resolved in the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 21.1

Customer Service Request Numbers	
00539610	00545866

1.6. Software Patches Included in this Release

The following software patches are included in this release:

Table 2. Software Patches Included in the Intel FPGA SDK for OpenCL Version 21.1

Software Version	Patch	Customer Service Request Number
Intel FPGA SDK for OpenCL Version 21.1	0.14cl	-

1.7. Intel FPGA SDK for OpenCL Pro Edition Release Notes Archives

If the table does not list a software version, the user guide for the previous software version applies.

Intel Quartus Prime Version	User Guide
20.4	Intel FPGA SDK for OpenCL Pro Edition Version 20.4 Release Notes
20.3	Intel FPGA SDK for OpenCL Pro Edition Version 20.3 Release Notes
20.2	Intel FPGA SDK for OpenCL Pro Edition Version 20.2 Release Notes
20.1	Intel FPGA SDK for OpenCL Pro Edition Version 20.1 Release Notes
19.4	Intel FPGA SDK for OpenCL Pro Edition Version 19.4 Release Notes
19.3	Intel FPGA SDK for OpenCL Pro Edition Version 19.3 Release Notes
19.2	Intel FPGA SDK for OpenCL Pro Edition Version 19.2 Release Notes
19.1	Intel FPGA SDK for OpenCL Pro Edition Version 19.1 Release Notes
18.1	Intel FPGA SDK for OpenCL Pro Edition Version 18.1 Release Notes
18.0	Intel FPGA SDK for OpenCL Pro Edition Release Notes
17.1	Intel FPGA SDK for OpenCL Release Notes
17.0	Intel FPGA SDK for OpenCL Release Notes
16.1	Intel FPGA SDK for OpenCL Release Notes
16.0	Altera SDK for OpenCL Version 16.0 Release Notes
15.1	Altera SDK for OpenCL Version 15.1 Release Notes
15.0	Altera SDK for OpenCL Version 15.0 Release Notes

1.8. Document Revision History of the Intel FPGA SDK for OpenCL Pro Edition Release Notes

Document Version	Intel Quartus Prime Version	Changes
2021.05.20	21.1	Added patch details and error messages for the Intel Quartus Prime compilation failure.
2021.04.07	21.1	Added a known issue about Intel Quartus Prime compilation failure.
2021.03.29	21.1	Initial release.