



Intel[®] FPGA SDK for OpenCL[™] Pro Edition

Version 20.4 Release Notes

Updated for Intel[®] Quartus[®] Prime Design Suite: **20.4**



RN-OCL004 | 2020.12.14

Latest document on the web: [PDF](#) | [HTML](#)



Contents

1. Intel® FPGA SDK for OpenCL™ Pro Edition Version 20.4 Release Notes.....	3
1.1. New Features and Enhancements.....	3
1.2. Operating System Support.....	3
1.3. Changes to Software Behavior.....	3
1.4. Known Issues and Workarounds.....	3
1.5. Software Issues Resolved.....	5
1.6. Software Patches Included in this Release.....	5
1.7. Intel FPGA SDK for OpenCL Pro Edition Release Notes Archives.....	5
1.8. Document Revision History of the Intel FPGA SDK for OpenCL Pro Edition Release Notes.....	5



1. Intel® FPGA SDK for OpenCL™ Pro Edition Version 20.4 Release Notes

The *Intel® FPGA SDK for OpenCL™ Pro Edition Release Notes* provides late-breaking information about the Intel FPGA Software Development Kit (SDK) for OpenCL⁽¹⁾⁽²⁾ Pro Edition and the Intel FPGA Runtime Environment (RTE) for OpenCL Pro Edition Version 20.4.

1.1. New Features and Enhancements

The Intel FPGA SDK for OpenCL Pro Edition and the Intel FPGA RTE for OpenCL Pro Edition include the following new features:

- Enabled the `aoc` command option `-hyper-optimized-handshaking` for Intel Agilex™ device.

1.2. Operating System Support

Information about OS support for the Intel FPGA SDK for OpenCL is available on the Operating System Support page of the Intel FPGA website.

Related Information

[Operating System Support](#)

1.3. Changes to Software Behavior

No changes to the software behavior were made in the current release of the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL.

Related Information

[OpenCL 2.0 Headers](#)

1.4. Known Issues and Workarounds

This section provides information about known issues that affect the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 20.4.

-
- (1) OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission of the Khronos Group™.
 - (2) The Intel FPGA SDK for OpenCL is based on a published Khronos Specification, and has passed the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

*Other names and brands may be claimed as the property of others.



Description	Workaround
When compiling an OpenCL kernel containing calls to library functions containing HLS tasks, incremental compile may trigger recompilation for unaffected kernels.	No known workaround. However, this is not a functional bug. It may result in a more conservative incremental compile.
The emulator runtime emits an assertion error if a kernel is enqueued 16,000 times.	Do not enqueue a kernel more than 16,000 times.
OpenCL kernels with names longer than 61 characters might fail in the Intel Quartus® Prime Pro Edition compiler with an error similar to the following error: <pre>Error (16045): Instance "... <long_kernel_name>_cra_slave_inst" instantiates undefined entity "<long_kernel_name>_function_cra_slave" File: <filename> Line: <linenumber></pre>	Reduce the size of the OpenCL kernel name.
OpenCL kernel pipes cannot be passed as arguments in some cases. The symptom is the runtime receives a CL_INVALID_BUFFER_SIZE (-61) error when you enqueue your kernel.	Modify your design to use channels instead of pipes.
When alternatively using sub-buffers and their parent buffers, changes written to one might not be reflected in the other.	Unmapping and mapping a buffer forces the sub-buffers and their parent buffers to be synced. Unmapping and mapping a buffer between buffer uses should prevent this issue.

This section provides information about known issues that affect the current release of the Intel FPGA SDK for OpenCL Custom Platform Toolkit and Reference Platforms. These issues might also affect Custom Platforms you create for use with the Intel FPGA SDK for OpenCL.

Description	Workaround
For Windows, when the host application queries the number of devices, calls to <code>clGetDeviceIDs</code> return 128 devices regardless of the actual number of devices present. <i>Note:</i> You can find the actual available devices at the beginning of the device list returned by <code>clGetDeviceIDs</code> . This issue affects the Intel Arria® 10 GX FPGA Development Kit Reference Platform and the Intel Stratix® 10 GX FPGA Development Kit Reference Platform.	Perform one of the following workarounds: <ul style="list-style-type: none"> Rewrite the host application to limit the query for <code>clGetDeviceIDs</code> to the actual number of devices. Rewrite the host application to use <code>clGetDeviceInfo</code> to query which devices are available. Calling <code>clGetDeviceInfo</code> with the <code>CL_DEVICE_AVAILABLE</code> flag correctly reports that extraneous devices are unavailable. Rewrite the host application to only call <code>clCreateContext</code> with the actual number of devices. Calling <code>clCreateContext</code> with extraneous devices fails with the error <code>CL_DEVICE_NOT_AVAILABLE</code>. Set the environment variable <code>CL_OVERRIDE_NUM_DEVICES_INTELFPGA</code> to the correct number of devices. Doing so fixes the erroneous behavior of <code>clGetDeviceIDs</code>.

Latest Known Intel FPGA SDK for OpenCL Software Issues

For additional known issue information for the current Intel FPGA SDK for OpenCL version and for previous versions, refer to the Knowledge Base web page.

Related Information

[Knowledge Base](#)



1.5. Software Issues Resolved

No software issues were reported, corrected or otherwise resolved in the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 20.4.

1.6. Software Patches Included in this Release

No software patches included in this release.

1.7. Intel FPGA SDK for OpenCL Pro Edition Release Notes Archives

If the table does not list a software version, the user guide for the previous software version applies.

Intel Quartus Prime Version	User Guide
20.3	Intel FPGA SDK for OpenCL Pro Edition Version 20.3 Release Notes
20.2	Intel FPGA SDK for OpenCL Pro Edition Version 20.2 Release Notes
20.1	Intel FPGA SDK for OpenCL Pro Edition Version 20.1 Release Notes
19.4	Intel FPGA SDK for OpenCL Pro Edition Version 19.4 Release Notes
19.3	Intel FPGA SDK for OpenCL Pro Edition Version 19.3 Release Notes
19.2	Intel FPGA SDK for OpenCL Pro Edition Version 19.2 Release Notes
19.1	Intel FPGA SDK for OpenCL Pro Edition Version 19.1 Release Notes
18.1	Intel FPGA SDK for OpenCL Pro Edition Version 18.1 Release Notes
18.0	Intel FPGA SDK for OpenCL Pro Edition Release Notes
17.1	Intel FPGA SDK for OpenCL Release Notes
17.0	Intel FPGA SDK for OpenCL Release Notes
16.1	Intel FPGA SDK for OpenCL Release Notes
16.0	Altera SDK for OpenCL Version 16.0 Release Notes
15.1	Altera SDK for OpenCL Version 15.1 Release Notes
15.0	Altera SDK for OpenCL Version 15.0 Release Notes

1.8. Document Revision History of the Intel FPGA SDK for OpenCL Pro Edition Release Notes

Document Version	Intel Quartus Prime Version	Changes
2020.12.14	20.4	Initial release.