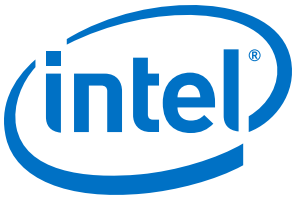

Intel® FPGA SDK for OpenCL™ Pro Edition

Version 20.3 Release Notes

Updated for Intel® Quartus® Prime Design Suite: **20.3**

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1. Intel® FPGA SDK for OpenCL™ Pro Edition Version 20.3 Release Notes

The *Intel® FPGA SDK for OpenCL™ Pro Edition Release Notes* provides late-breaking information about the Intel FPGA Software Development Kit (SDK) for OpenCL[1][2] Pro Edition and the Intel FPGA Runtime Environment (RTE) for OpenCL Pro Edition Version 20.3.

1.1. New Features and Enhancements

The Intel FPGA SDK for OpenCL Pro Edition and the Intel FPGA RTE for OpenCL Pro Edition include the following new features:

- Enhanced the high-level design report to include the Bottlenecks viewer. The Bottlenecks viewer works with the Loop Analysis, Schedule Viewer, and Graphics Viewer, and reports the throughput bottlenecks.
- Enhanced loop fusion to support fusing loops with different trip counts. In previous compiler versions, only loops with the same trip count would be considered for fusing.

  The Intel FPGA SDK for OpenCL only considers adjacent loops with same trip count for automatic loop fusion. Use the `loop_fuse` pragma to inform the compiler to consider adjacent loops with different trip counts for fusing.
- Included Microsoft Visual Studio* 2017 and 2019 and Eclipse* plug-ins in the Intel FPGA SDK for OpenCL.
- Removed the Intel FPGA dynamic profiler for OpenCL GUI and integrated it with the Intel VTune Profiler to view the kernel performance data.
- Enhanced the Intel VTune Profiler to support the following:
  - Temporal counters that can report profile data over the time.
  - Shared counters to allow reducing area overhead during the profiler runs, at the expense of more time required to collect profile data.
  - New counters to report channel idle time, average and maximum channel depth, and LSU idle time.

(1) OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission of the Khronos Group™.

(2) The Intel FPGA SDK for OpenCL is based on a published Khronos Specification, and has passed the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.

1.2. Operating System Support

Information about OS support for the Intel FPGA SDK for OpenCL is available on the Operating System Support page of the Intel FPGA website.

Related Information

Operating System Support

1.3. Changes to Software Behavior

Items listed in the following table represent cases in which the behaviors of the current release of the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL differ from the previous version.

Description	Required Actions
The `-fpc` aoc command option is removed.	Use the `-ffp-contract=fast` command option instead.
The `-fp-relaxed` aoc command option is removed.	Use the `-ffp-reassoc` command option instead.
Support for the Legacy Emulator is removed.	-
The offline compiler now exits and returns an error message when it detects an irreducible loop. Previously, the compiler would exit without an error message.	-
Support for Red Hat Enterprise Linux* Server 6 is removed.	-
The Intel FPGA dynamic profiler for OpenCL GUI is removed.	Use the enhanced Intel VTune Profiler to view the performance data of your kernel.
Support for Windows and Linux BSPs is removed.	Use version 20.2 or older BSPs available at Download Center for FPGAs as a reference. If you want to migrate your BSP to a newer version, follow the recommended steps provided in the Reference Platform Porting Guides available under Intel FPGA SDK for OpenCL documentation.

Related Information

OpenCL 2.0 Headers

1.4. Known Issues and Workarounds

This section provides information about known issues that affect the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 20.3.

Description	Workaround
When compiling an OpenCL kernel containing calls to library functions containing HLS tasks, incremental compile may trigger recompilation for unaffected kernels.	No known workaround. However, this is not a functional bug. It may result in a more conservative incremental compile.
The emulator runtime emits an assertion error if a kernel is enqueued 16,000 times.	Do not enqueue a kernel more than 16,000 times.
OpenCL kernels with names longer than 61 characters might fail in the Intel Quartus® Prime Pro Edition compiler with an error similar to the following error: `Error (16045): Instance "...|<long_kernel_name>_cra_slave_inst" instantiates undefined entity`	Reduce the size of the OpenCL kernel name.

continued...

Description	Workaround
`"<long_kernel_name>_function_cra_slave" File: <filename> Line: <linenumber>`	
OpenCL kernel pipes cannot be passed as arguments in some cases. The symptom is the runtime receives a `CL_INVALID_BUFFER_SIZE (-61)` error when you enqueue your kernel.	Modify your design to use channels instead of pipes.
When alternatively using sub-buffers and their parent buffers, changes written to one might not be reflected in the other.	Unmapping and mapping a buffer forces the sub-buffers and their parent buffers to be synced. Unmapping and mapping a buffer between buffer uses should prevent this issue.

This section provides information about known issues that affect the current release of the Intel FPGA SDK for OpenCL Custom Platform Toolkit and Reference Platforms. These issues might also affect Custom Platforms you create for use with the Intel FPGA SDK for OpenCL.

Description	Workaround
For Windows, when the host application queries the number of devices, calls to `clGetDeviceIDs` return 128 devices regardless of the actual number of devices present. *Note:* You can find the actual available devices at the beginning of the device list returned by `clGetDeviceIDs`. This issue affects the Intel Arria® 10 GX FPGA Development Kit Reference Platform and the Intel Stratix® 10 GX FPGA Development Kit Reference Platform.	Perform one of the following workarounds: • Rewrite the host application to limit the query for `clGetDeviceIDs` to the actual number of devices. • Rewrite the host application to use `clGetDeviceInfo` to query which devices are available. Calling `clGetDeviceInfo` with the `CL_DEVICE_AVAILABLE` flag correctly reports that extraneous devices are unavailable. • Rewrite the host application to only call `clCreateContext` with the actual number of devices. Calling `clCreateContext` with extraneous devices will fail with the error `CL_DEVICE_NOT_AVAILABLE`. • Set the environment variable *`CL_OVERRIDE_NUM_DEVICES_INTELFPGA`* to the correct number of devices. Doing so fixes the erroneous behavior of `clGetDeviceIDs`.

Latest Known Intel FPGA SDK for OpenCL Software Issues

For additional known issue information for the current Intel FPGA SDK for OpenCL version and for previous versions, refer to the Knowledge Base web page.

Related Information

Knowledge Base

1.5. Software Issues Resolved

The following issues were corrected or otherwise resolved in the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 20.3.

Table 1. Issues Resolved in the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 20.3

Customer Service Request Numbers	
00461444	11370544
00494725	00492598
00501613	00536122

1.6. Software Patches Included in this Release

No software patches included in this release.

1.7. Intel FPGA SDK for OpenCL Pro Edition Release Notes Archives

If the table does not list a software version, the user guide for the previous software version applies.

Intel Quartus Prime Version	User Guide
20.2	Intel FPGA SDK for OpenCL Pro Edition Version 20.2 Release Notes
20.1	Intel FPGA SDK for OpenCL Pro Edition Version 20.1 Release Notes
19.4	Intel FPGA SDK for OpenCL Pro Edition Version 19.4 Release Notes
19.3	Intel FPGA SDK for OpenCL Pro Edition Version 19.3 Release Notes
19.2	Intel FPGA SDK for OpenCL Pro Edition Version 19.2 Release Notes
19.1	Intel FPGA SDK for OpenCL Pro Edition Version 19.1 Release Notes
18.1	Intel FPGA SDK for OpenCL Pro Edition Version 18.1 Release Notes
18.0	Intel FPGA SDK for OpenCL Pro Edition Release Notes
17.1	Intel FPGA SDK for OpenCL Release Notes
17.0	Intel FPGA SDK for OpenCL Release Notes
16.1	Intel FPGA SDK for OpenCL Release Notes
16.0	Altera SDK for OpenCL Version 16.0 Release Notes
15.1	Altera SDK for OpenCL Version 15.1 Release Notes
15.0	Altera SDK for OpenCL Version 15.0 Release Notes

1.8. Document Revision History of the Intel FPGA SDK for OpenCL Pro Edition Release Notes

Document Version	Intel Quartus Prime Version	Changes
2020.09.23	20.3	Initial release.