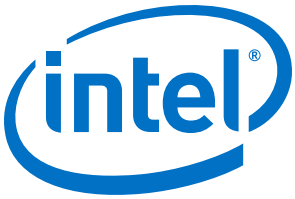

Intel® FPGA SDK for OpenCL™ Pro Edition

Version 20.1 Release Notes

Updated for Intel® Quartus® Prime Design Suite: **20.1**

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1. Intel® FPGA SDK for OpenCL™ Pro Edition Version 20.1 Release Notes

The *Intel® FPGA SDK for OpenCL™ Pro Edition Release Notes* provides late-breaking information about the Intel FPGA Software Development Kit (SDK) for OpenCL[1][2] Pro Edition and the Intel FPGA Runtime Environment (RTE) for OpenCL Pro Edition Version 20.1.

1.1. New Features and Enhancements

The Intel FPGA SDK for OpenCL Pro Edition and the Intel FPGA RTE for OpenCL Pro Edition include the following new features:

- Removed `numreadports` and `numwriteports` kernel memory attributes.
- Deprecated the memory attribute `max_concurrency` and might be removed from a future version. Use the `private_copies` attribute instead, which achieves the exact same thing.
- Added support for sharing multiple devices across multiple host programs.
- Added a new memory attribute `force_pow2_depth` to control padding of on-chip memories.
- Changed the default work group size for kernels with barriers from 256 to 128.
- Added support for emulating applications with a channel that reads or writes to an I/O channel.
- Added the `loop_fuse` pragma to direct the offline compiler to fuse adjacent loops into a single loop without affecting either loop's functionality.
- Added the `nofusion` pragma to direct the offline compiler to avoid fusing the annotated loop with any of the adjacent loops.
- Changed the memory attribute `max_concurrency` to `private_copies`.
- Changed the `aoc` command option `-fmax=<fmax target in MHz>` to `-clock=<clock target in Hz/KHz/MHz/GHz or s/ms/us/ns/ps>`.
- Removed the `aoc` command option `-duplicate-ring`.
- Added the `-force-single-store-ring` `aoc` command option to narrow the global memory interconnect to save area while limiting write-only throughput that is one bank worth.

(1) OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission of the Khronos Group™.

(2) The Intel FPGA SDK for OpenCL is based on a published Khronos Specification, and has passed the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.

- Added the `-num-reorder=N` `aoc` command option to narrow the global memory interconnect in order to save area while reducing read-only throughput.
- Enhanced the Summary report to provide more information in the order of compilation.
- Deprecated the Fmax II report and merged it with the Loops Analysis report.
- Removed the cluster-level latency from the Schedule Viewer report.
- Enhanced the Scheduler Viewer report to show three types of loop bottleneck, such as f_{max}/II bottlenecks, memory dependency, and occupancy limiter.
- Enhanced component throughput with automated loop fusion, which reduces the number of loop control structures needed in your component.

1.2. Operating System Support

Information about OS support for the Intel FPGA SDK for OpenCL is available on the Operating System Support page of the Intel FPGA website.

Related Information

Operating System Support

1.3. Changes to Software Behavior

Items listed in the following table represent cases in which the behaviors of the current release of the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL differ from the previous version.

Description	Required Actions
The Intel FPGA SDK for OpenCL Offline Compiler version 20.1 sometimes reduces the number of speculated iterations of a loop when compared to the previous releases. This reduction in the number of speculated iterations does not affect the loop's initiation interval or the design's f_{max}. The offline compiler applies this new optimization only if the loop does not have a `speculated_iterations` pragma applied.	Remove the existing use of the `speculated_iterations` pragma in your design. This may result in better QoR since the same II and f_{max} may be achieved with fewer speculated iterations. This recommendation applies only when targeting Intel Stratix® 10 devices.

Related Information

OpenCL 2.0 Headers

1.4. Known Issues and Workarounds

This section provides information about known issues that affect the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 20.1.

Description	Workaround
When compiling an OpenCL kernel containing calls to library functions containing HLS tasks, incremental compile may trigger recompilation for unaffected kernels.	No known workaround. However, this is not a functional bug. It may result in a more conservative incremental compile.
In the Loop Analysis HTML report, if the Loop List pane shows a partially unrolled loop, the corresponding loop information does not show up in the Loop Analysis table.	Perform this steps: 1. Navigate to the following folder:

continued...

Description	Workaround
	`<compilation object name>/reports/lib/json` 2. Open the `loops.json` file and search the loop name for information about II, speculated iterations, and source location. 3. Open the `fmax_ii.json` file and search the loop name without "Partially unrolled" for information about scheduled f_{max}, maximum interleaving iterations, and latency.

Loop fusion may cause the compiler to crash when one (or more) loops are contained within conditional statements, and the value of the condition is computed in the previous loop.
For example:
`bool repeated;`
`for (int i = 0; i < N; ++i) {`
`  if (i+1 < N) {`
`  repeated = data[i] == data[i+1];`
`  }`
`}`
`if (repeated)`
`{`
`  for (int i = 0; i < N; ++i)`
`  {`
`  int val = data[i];`
`  data2[val][i] += value[i];`
`  }`
`}`
	Mark one of the loops with `#pragma nofusion`.

Using HLS streams in HLS System-Of-Tasks (SOT) in OpenCL library does not work with hyper-optimized-handshaking protocol when targeting Intel Stratix 10 devices, and results in the following error: `internal compiler error: node internal validation failed`	Turn off the protocol by setting `-hyper-optimized-handshaking=off`.
In the fast emulator, the memory used for modeling channel depth scales differently than under the legacy emulator. This means that some designs (that compile for the legacy emulator) fail to compile for the fast emulator and display the following warning and error message: `*Internal compiler error* Unable to allocate section memory!`	If possible, scale down the design or limit the channel depth.
The emulator runtime emits an assertion error if a kernel is enqueued 16,000 times.	Do not enqueue a kernel more than 16,000 times.

OpenCL kernels with names longer than 61 characters might fail in the Intel Quartus® Prime Pro Edition compiler with an error similar to the following error:
`Error (16045): Instance "...|`
`<long_kernel_name>_cra_slave_inst" instantiates`
`undefined entity`
`"<long_kernel_name>_function_cra_slave" File:`
`<filename> Line:`
`<linenumber>`
	Reduce the size of the OpenCL kernel name.

continued...

Description	Workaround
OpenCL kernel pipes cannot be passed as arguments in some cases. The symptom is the runtime receives a `CL_INVALID_BUFFER_SIZE (-61)` error when you enqueue your kernel.	Modify your design to use channels instead of pipes.
When alternatively using sub-buffers and their parent buffers, changes written to one might not be reflected in the other.	Unmapping and mapping a buffer forces the sub-buffers and their parent buffers to be synced. Unmapping and mapping a buffer between buffer uses should prevent this issue.
In the OpenCL runtime, making more than one OpenCL context in a multithreaded environment might cause a segmentation fault.	—

This section provides information about known issues that affect the current release of the Intel FPGA SDK for OpenCL Custom Platform Toolkit and Reference Platforms. These issues might also affect Custom Platforms you create for use with the Intel FPGA SDK for OpenCL.

Description	Workaround
Race conditions can occur between enqueue and dequeue buffer operations and host pipe operations. These conditions can results in incorrect data being read or written.	Manually make sure that no enqueue or dequeue buffer operations occur in parallel with host pipe API calls. A way to ensure that buffer operations do not occur in parallel with host pipe API calls is to do buffer operations as blocking calls before the first host pipe operation and after you are certain that the last host pipe operation has been completed (for example, all the data is read back).
For Windows, when the host application queries the number of devices, calls to `clGetDeviceIDs` return 128 devices regardless of the actual number of devices present. *Note:* You can find the actual available devices at the beginning of the device list returned by `clGetDeviceIDs`. This issue affects the Intel Arria® 10 GX FPGA Development Kit Reference Platform and the Intel Stratix 10 GX FPGA Development Kit Reference Platform.	Perform one of the following workarounds: • Rewrite the host application to limit the query for `clGetDeviceIDs` to the actual number of devices. • Rewrite the host application to use `clGetDeviceInfo` to query which devices are available. Calling `clGetDeviceInfo` with the `CL_DEVICE_AVAILABLE` flag correctly reports that extraneous devices are unavailable. • Rewrite the host application to only call `clCreateContext` with the actual number of devices. Calling `clCreateContext` with extraneous devices will fail with the error `CL_DEVICE_NOT_AVAILABLE`. • Set the environment variable *`CL_OVERRIDE_NUM_DEVICES_INTELFPGA`* to the correct number of devices. Doing so fixes the erroneous behavior of `clGetDeviceIDs`.

Latest Known Intel FPGA SDK for OpenCL Software Issues

For additional known issue information for the current Intel FPGA SDK for OpenCL version and for previous versions, refer to the Knowledge Base web page.

Related Information

Knowledge Base

1.5. Software Issues Resolved

The following issues were corrected or otherwise resolved in the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 20.1.

Table 1. Issues Resolved in the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 20.1

Customer Service Request Numbers				
00454036	00448582	00462192	00482683	00284692

1.6. Software Patches Included in this Release

The following software patches are included in this release:

Table 2. Software Patches Included in the Intel FPGA SDK for OpenCL

Software Version	Patch	Customer Service Request Number
Intel FPGA SDK for OpenCL Version 20.1	0.07cl	-
	0.10cl	-

1.7. Intel FPGA SDK for OpenCL Pro Edition Release Notes Archives

If the table does not list a software version, the user guide for the previous software version applies.

Intel Quartus Prime Version	User Guide
19.4	Intel FPGA SDK for OpenCL Pro Edition Version 19.4 Release Notes
19.3	Intel FPGA SDK for OpenCL Pro Edition Version 19.3 Release Notes
19.2	Intel FPGA SDK for OpenCL Pro Edition Version 19.2 Release Notes
19.1	Intel FPGA SDK for OpenCL Pro Edition Version 19.1 Release Notes
18.1	Intel FPGA SDK for OpenCL Pro Edition Version 18.1 Release Notes
18.0	Intel FPGA SDK for OpenCL Pro Edition Release Notes
17.1	Intel FPGA SDK for OpenCL Release Notes
17.0	Intel FPGA SDK for OpenCL Release Notes
16.1	Intel FPGA SDK for OpenCL Release Notes
16.0	Altera SDK for OpenCL Version 16.0 Release Notes
15.1	Altera SDK for OpenCL Version 15.1 Release Notes
15.0	Altera SDK for OpenCL Version 15.0 Release Notes

1.8. Document Revision History of the Intel FPGA SDK for OpenCL Pro Edition Release Notes

Document Version	Intel Quartus Prime Version	Changes
2020.04.13	20.1	Initial release.