



Intel[®] FPGA SDK for OpenCL[™] Pro Edition

Version 19.2 Release Notes

Updated for Intel[®] Quartus[®] Prime Design Suite: **19.2**



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1. Intel® FPGA SDK for OpenCL™ Pro Edition Version 19.2 Release Notes

The *Intel® FPGA SDK for OpenCL™ Pro Edition Release Notes* provides late-breaking information about the Intel FPGA Software Development Kit (SDK) for OpenCL⁽¹⁾⁽²⁾ Pro Edition and the Intel FPGA Runtime Environment (RTE) for OpenCL Pro Edition Version 19.2.

1.1. New Features and Enhancements

The Intel FPGA SDK for OpenCL Pro Edition and the Intel FPGA RTE for OpenCL Pro Edition include the following new features:

- By default, the Intel FPGA SDK for OpenCL Offline Compiler targets the Fast Emulator when you use the `-march=emulator` flag. For more information about emulating your OpenCL kernel, refer to [Emulating and Debugging Your OpenCL Kernel](#) in the *Intel FPGA SDK for OpenCL Programming Guide*.

The Legacy Emulator is still available and you can target it by using a combination of `-march=emulator -legacy-emulator` flags. For more information, refer to [Using the Legacy Emulator](#) in the *Intel FPGA SDK for OpenCL Programming Guide*.

- The limit for maximum number of declared variables in the local memory per kernel is increased to 512.
- Added `disable_loop_pipelining` pragma to direct the Intel FPGA SDK for OpenCL Offline Compiler to disable loop pipelining.
- In the high-level design (`report.html`) report, the System Viewer, Block Viewer, and Cluster Viewer have been merged into a hierarchical Graph Viewer.

1.2. Operating System Support

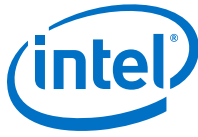
Information about OS support for the Intel FPGA SDK for OpenCL is available on the Operating System Support page of the Intel FPGA website.

Related Information

[Operating System Support](#)

(1) OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission of the Khronos Group™.

(2) The Intel FPGA SDK for OpenCL is based on a published Khronos Specification, and has passed the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.



1.3. Changes to Software Behavior

Items listed in the following table represent cases in which the behaviors of the current release of the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL differ from the previous version.

Description	Required Actions
The OpenCL headers provided by the Intel FPGA SDK for OpenCL have been updated to the latest version distributed by Khronos.	Refer to the OpenCL 2.0 Headers in the <i>Intel FPGA SDK for OpenCL Pro Edition: Programming Guide</i> for more information.
The <code>cl.hpp</code> header is now deprecated.	Update your OpenCL host program code to use the <code>cl2.hpp</code> header that supports all versions of OpenCL.
The OpenCL host runtime now returns <code>CL_PROFILING_INFO_NOT_AVAILABLE</code> when you call <code>clGetEventProfilingInfo</code> function on a <code>cl_event</code> associated with a <code>cl_command_queue</code> that was not created with the <code>CL_QUEUE_PROFILING_ENABLE</code> property. Previous versions of the Intel FPGA SDK for OpenCL did not enforce this requirement of the OpenCL Specification version 1.2.	Update your OpenCL host program to create the <code>cl_command_queue</code> with the <code>CL_PROFILING_INFO_ENABLE</code> property if you want to enable profiling.
The formatting of <code>printf</code> command output of OpenCL vector types has been modified to be conformant with the OpenCL Specification version 1.2.	—
Mandatory requirement for all host programs that use Intel FPGA-specific APIs and enumerations.	If your host programs use Intel FPGA-specific APIs and enumerations, such as <code>clReadPipeIntelFPGA</code> , <code>clGetProfileInfoIntelFPGA</code> , and other APIs that end with <code>IntelFPGA</code> , you must explicitly include the <code>CL/cl_ext_intelfpga.h</code> header file in your source code.
The host pipe feature requires the use of OpenCL 2.0 features.	Enable support for OpenCL 2.0 APIs in all of your host programs that use host pipes in their source code. Refer to the OpenCL 2.0 Headers in the <i>Intel FPGA SDK for OpenCL Pro Edition: Programming Guide</i> for more information.
In previous versions of Intel FPGA SDK for OpenCL, the offline compiler automatically disabled the local memory replication for all memory systems if it estimated an M20K utilization of over 100%. The offline compiler no longer disables the local memory replication automatically.	To restore the behavior of disabling the local memory replication automatically, use the <code>-no-local-memory-replication</code> option in the <code>aoc</code> command.
Automatic loop unrolling is now disabled.	If you want to enable it, use LLVM options <code>-unroll-threshold</code> and <code>-unroll-partial-threshold</code> in the <code>aoc</code> command. Recommended settings: <ul style="list-style-type: none"> For optimization levels <code>-O0</code>, <code>-O1</code>, and <code>-O2</code>, set <code>-unroll-threshold=150</code> and <code>-unroll-partial-threshold=150</code>. For optimization level <code>-O3</code>, set <code>-unroll-threshold=300</code> and <code>-unroll-partial-threshold=150</code>.
Support for passing pipes or channels by reference is removed.	Update your code to pass pipes or channels by value.
The <code>restrict</code> keyword is renamed to <code>__restrict</code> .	Update your code to use the <code>__restrict</code> keyword instead of the <code>restrict</code> keyword.

Items listed in the following table represent cases in which the behaviors of the current release of the Intel FPGA SDK for OpenCL Custom Platform Toolkit and Reference Platforms differ from the previous version.



Description	Workaround
N/A	N/A

Related Information

[OpenCL 2.0 Headers](#)

1.4. Known Issues and Workarounds

This section provides information about known issues that affect the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 19.2.

Description	Workaround
In the fast emulator, the memory used for modeling channel depth scales differently than under the legacy emulator. This means that some designs (that can be compiled for the legacy emulator) fail to compile for the fast emulator and display the following warning and error message: *Internal compiler error* Unable to allocate section memory!	If possible, scale down the design or limit the channel depth. If everything else fails, use the legacy emulator.
The OpenCL emulator does not return <code>CL_INVALID_GLOBAL_OFFSET</code> when a kernel with the <code>uses_global_work_offset(0)</code> kernel attribute set is enqueued with a non-zero or non-NULL <code>global_work_offset</code> argument.	Set the <code>global_work_offset</code> argument to NULL or zero in all work group dimensions so that this issue does not change the kernel output between the emulator and hardware.
OpenCL kernels with names longer than 61 characters might fail in the Intel Quartus® Prime Pro Edition compiler with an error similar to the following error: <pre>Error (16045): Instance "... <long_kernel_name>_cra_slave_inst" instantiates undefined entity "<long_kernel_name>_function_cra_slave" File: <filename> Line: <linenumber></pre>	Reduce the size of the OpenCL kernel name.
Valid OpenCL kernel pipes cannot be passed as arguments in some cases. The symptom is the runtime will receive a <code>CL_INVALID_BUFFER_SIZE (-61)</code> error when you enqueue your kernel.	Modify your design to use channels instead of pipes.
The emulator runtime results in an assertion error if a kernel is enqueued 16,000 times.	Do not enqueue a kernel more than 16,000 times.
When alternatively using sub-buffers and their parent buffers, changes written to one might not be reflected in the other.	Unmapping and mapping a buffer forces the sub-buffers and their parent buffers to be synced. Unmapping and mapping a buffer between buffer uses should prevent this issue.
In the OpenCL runtime, making more than one OpenCL context in a multithreaded environment might cause a segmentation fault.	—

This section provides information about known issues that affect the current release of the Intel FPGA SDK for OpenCL Custom Platform Toolkit and Reference Platforms. These issues might also affect Custom Platforms you create for use with the Intel FPGA SDK for OpenCL.

Description	Workaround
Race conditions can occur between enqueue and dequeue buffer operations and host pipe operations. These conditions can result in incorrect data being read or written.	Manually make sure that no enqueue or dequeue buffer operations occur in parallel with host pipe API calls.

continued...



Description	Workaround
	A way to ensure that buffer operations do not occur in parallel with host pipe API calls is to do buffer operations as blocking calls before the first host pipe operation and after you are certain that the last host pipe operation has been completed (for example, all the data is read back).
<p>For Windows, when the host application queries the number of devices, calls to <code>clGetDeviceIDs</code> return 128 devices regardless of the actual number of devices present.</p> <p><i>Note:</i> You can find the actual available devices at the beginning of the device list returned by <code>clGetDeviceIDs</code>.</p> <p>This issue affects the Intel Arria® 10 GX FPGA Development Kit Reference Platform and the Intel Stratix® 10 GX FPGA Development Kit Reference Platform.</p>	<p>Perform one of the following workarounds:</p> <ul style="list-style-type: none"> • Rewrite the host application to limit the query for <code>clGetDeviceIDs</code> to the actual number of devices. • Rewrite the host application to use <code>clGetDeviceInfo</code> to query which devices are available. Calling <code>clGetDeviceInfo</code> with the <code>CL_DEVICE_AVAILABLE</code> flag correctly reports that extraneous devices are unavailable. • Rewrite the host application to only call <code>clCreateContext</code> with the actual number of devices. Calling <code>clCreateContext</code> with extraneous devices will fail with the error <code>CL_DEVICE_NOT_AVAILABLE</code>. • Set the environment variable <code>CL_OVERRIDE_NUM_DEVICES_INTELFPGA</code> to the correct number of devices. Doing so fixes the erroneous behavior of <code>clGetDeviceIDs</code>.

Latest Known Intel FPGA SDK for OpenCL Software Issues

For additional known issue information for the current Intel FPGA SDK for OpenCL version and for previous versions, refer to the Knowledge Base web page.

Related Information

[Knowledge Base](#)

1.5. Software Issues Resolved

No software issues were reported, corrected or otherwise resolved in the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 19.2.

1.6. Software Patches Included in this Release

The following software patch is included in this release:

Table 2. Software Patches Included in the Intel FPGA SDK for OpenCL

Software Version	Patch	Customer Service Request Number
Intel FPGA SDK for OpenCL Version 19.2	0.12cl	-

1.7. Intel FPGA SDK for OpenCL Pro Edition Release Notes Archives

If the table does not list a software version, the user guide for the previous software version applies.

Intel Quartus Prime Version	User Guide
19.1	Intel FPGA SDK for OpenCL Pro Edition Version 19.1 Release Notes
18.1	Intel FPGA SDK for OpenCL Pro Edition Version 18.1 Release Notes
<i>continued...</i>	



Intel Quartus Prime Version	User Guide
18.0	Intel FPGA SDK for OpenCL Pro Edition Release Notes
17.1	Intel FPGA SDK for OpenCL Release Notes
17.0	Intel FPGA SDK for OpenCL Release Notes
16.1	Intel FPGA SDK for OpenCL Release Notes
16.0	Altera SDK for OpenCL Version 16.0 Release Notes
15.1	Altera SDK for OpenCL Version 15.1 Release Notes
15.0	Altera SDK for OpenCL Version 15.0 Release Notes

1.8. Document Revision History of the Intel FPGA SDK for OpenCL Pro Edition Release Notes

Document Version	Intel Quartus Prime Version	Changes
2019.07.01	19.2	Initial release.