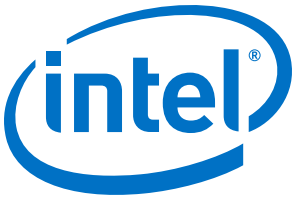

Intel® FPGA SDK for OpenCL™

Release Notes

Updated for Intel® Quartus® Prime Design Suite: **17.1**

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1 Intel® FPGA SDK for OpenCL™ Version 17.1 Release Notes

The *Intel® FPGA SDK for OpenCL™ Release Notes* provides late-breaking information about the Intel Software Development Kit (SDK) for OpenCL[1][2] and the Intel FPGA Runtime Environment (RTE) for OpenCL Version 17.1.

1.1 New Features and Enhancements

The Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 17.1 include the following new features:

- New execution and static analysis reports.
- Initial Intel Stratix® 10 optimization and support
- Removed requirement for Intel FPGA SDK for OpenCL license.
  - You can also now run your OpenCL kernel without a paid runtime license
- Improved Profiler that highlights high-stall percentages.
- New `-fast-compile` option for the offline compiler, supported for Intel Arria® 10 and newer device families.

(1) OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission of the Khronos Group™.

(2) The Intel FPGA SDK for OpenCL is based on a published Khronos Specification, and has passed the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.

- New direct communication with kernels via host pipes. Use the new `cl_intel_fpga_host_pipe` extension to enable point-to-point pipe communication between a kernel and the host program.
- Updates to `aoc` and `aocl` command options to improve the use model.
- Product rebranding:
  - Changed the following variable, parameter, and macro names:
    - `ALTERA_CL` is now `INTELFPGA_CL`
    - `ALTERAOCLSDKROOT` is now `INTELFPGAOCLSDKROOT`
    - `CL_CONTEXT_COMPILER_MODE_ALTERA` is now `CL_CONTEXT_COMPILER_MODE_INTELFPGA`
    - `CL_CONTEXT_EMULATOR_DEVICE_ALTERA` is now `CL_CONTEXT_EMULATOR_DEVICE_INTELFPGA`
    - `CL_CONTEXT_PROGRAM_VARIABLES_TOTAL_SIZE_ALTERA` is now `CL_CONTEXT_PROGRAM_VARIABLES_TOTAL_SIZE_INTELFPGA`
  - Changed the following API and function names:
    - `clGetExtensionFunctionAddress` is now `clGetExtensionFunctionAddressIntelFPGA`
    - `write_channel_altera` is now `write_channel_intel`
    - `write_channel_nb_altera` is now `write_channel_nb_intel`

1.2 Operating System Support

Information about OS support for the Intel FPGA SDK for OpenCL is available on the Operating System Support page of the Altera website.

Related Links

Operating System Support

1.3 Changes to Software Behavior

Items listed in the following table represent cases in which the behaviors of the current release of the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL differ from the previous version.

Description	Workaround
The format of compiler command options changed to use a single dash instead of a double-dash. For example: • `--help` is now `-help` • `--list-boards` is now `-list-boards` Also, command options that take a parameter now use an equal sign (=) to specify the option parameter instead of separating the option and parameter with a space. For example: • `--board <board_name>` is now `-board=<board_name>` • `--no-interleaving <global_memory_type>` is now `-no-interleaving=<global_memory_type>`	The old format of the compiler command options are deprecated, but still work. However, these options might be removed in a future release of the Intel FPGA SDK for OpenCL. If you have any scripts that use the old option format, migrate your scripts to use the new option format to prevent any problems when the old format options are removed.

Items listed in the following table represent cases in which the behaviors of the current release of the Intel FPGA SDK for OpenCL Custom Platform Toolkit and Reference Platforms differ from the previous version.

Description	Workaround
N/A	N/A

1.4 Known Issues and Workarounds

This section provides information about known issues that affect the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 17.1.

Description	Workaround
OpenCL kernels with names longer than 61 characters might fail in the Quartus compiler with an error similar to the following error: `Error (16045): Instance "...|<long_kernel_name>_cra_slave_inst" instantiates undefined entity "<long_kernel_name>_function_cra_slave" File: <filename> Line: <linenumber>`	Reduce the size of the OpenCL kernel name.
Valid OpenCL kernel pipes cannot be passed as arguments in some cases. The symptom is the runtime will receive a `CL_INVALID_BUFFER_SIZE (-61)` error when you enqueue your kernel.	Modify your design to use channels instead of pipes.
The emulator runtime results in an assertion error if a kernel is enqueued 16,000 times.	Do not enqueue a kernel more than 16,000 times.
OpenCL design kernel source files cannot be named `kernel.cl`.	Rename your kernel source file.
When alternatively using subbuffers and their parent buffers, changes written to one might not be reflected in the other.	Unmapping and mapping a buffer forces the subbuffers and their parent buffers to be synced. Unmapping and mapping a buffer between buffer uses should prevent this issue.
The OpenCL Profiler does not support kernels with multiple channel call sites. If you try to use the Profiler on such a kernel, you get the following compilation error: `******* Error: Assert failure at Pass_InsertProfilerHardware.cpp(274) ******* extsig_list.end() != it && (*it)->has_interface_spec() FAILED`	Avoid using the OpenCL Profiler on a kernel that contains multiple channel call sites.

This section provides information about known issues that affect the current release of the Intel FPGA SDK for OpenCL Custom Platform Toolkit and Reference Platforms. These issues might also affect Custom Platforms you create for use with the Intel FPGA SDK for OpenCL.

Description	Workaround
Race conditions can occur between enqueue and dequeue buffer operations and host pipe operations. These conditions can results in incorrect data being read or written.	Manually make sure that no enqueue or dequeue buffer operations occur in parallel with host pipe API calls. A way to ensure that buffer operations to do not occur in parallel with host pipe API calls is to do buffer operations as blocking calls before the first host pipe operation and after you are certain that the last host pipe operation has been completed (for example, all the data is read back).

For additional known issue information for the current Intel FPGA SDK for OpenCL version, refer to the Knowledge Base web page.

Additional Known Software Issues Affecting the Intel FPGA SDK for OpenCL Version 17.1

Latest Known Intel FPGA SDK for OpenCL Software Issues

You can find known issue information for previous Intel FPGA SDK for OpenCL versions on the Knowledge Base web page.

Related Links

Knowledge Base

1.5 Software Issues Resolved

The following issues were corrected or otherwise resolved in the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 17.1.

Table 1. Issues Resolved in the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 17.1

Customer Service Request Numbers						
11035424	11301583	11303204	11308240	11308453	11311932	11316182
11316480	11318255	11320806	11320877	11323078	11323330	11324191
11325215	11325284	11328711	11329325	11330453	11334800	11335141

1.6 Software Patches Included in this Release

Table 2. Software Patches Included in the Intel FPGA SDK for OpenCL Version 17.1

Software Version	Patch	Customer Service Request Number
Intel FPGS SDK for OpenCL version 17.0.2	2.02cl	11323352
Intel FPGA SDK for OpenCL version 17.0.1	1.02cl	11329010
Altera SDK for OpenCL version 16.0.2	2.35cl	11303204

1.7 Document Revision History

Table 3. Intel FPGA SDK for OpenCL Version 17.1 Release Notes Document Revision History

Date	Document Version	Changes
November 2017	2017.11.04	• Initial release.