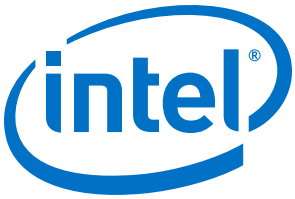

Intel® FPGA SDK for OpenCL

Release Notes

RN-OCL004
2017.05.08

Last updated for Intel® Quartus® Prime Design Suite: 17.0

Subscribe
Send Feedback

Contents

1 Intel® FPGA SDK for OpenCL™ Version 17.0 Release Notes

The *Intel® FPGA SDK for OpenCL™ Release Notes* provides late-breaking information about the Intel Software Development Kit (SDK) for OpenCL[1][2] and the Intel FPGA Runtime Environment (RTE) for OpenCL Version 17.0.

1.1 New Features and Enhancements

The Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 17.0 include the following new features:

- Support for compiling encrypted OpenCL code that is provided to you. Compiling code that you encrypt yourself is not supported.
- Ubuntu Linux operating system support.
- Enhanced loop optimization with the `#pragma loop_coalesce` and `#pragma ii` compiler directives.
- Support for arbitrary precisions integers up to 64 bits wide.
- Improved emulation support:
  - New emulation support for I/O channels.
  - New `--emulator-channel-depth-model` compiler option to control how closely emulation channel depth matches hardware channel depth.
  - New emulation support for `autorun` kernel attribute.
- New features in kernel report (`report.html`) viewer:
  - New summary page.
  - New component memory viewer.

1 OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission of the Khronos Group™.

2 The Intel FPGA SDK for OpenCL is based on a published Khronos Specification, and has passed the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.

- New `bank_bits` attribute to specify bits from a memory address to use as bank-select bits.
- Updated Profiler GUI with tab to display source code. Profiler command has additional optional source code file parameter.
- Product rebranding:
  - Altera Client Driver (ACD) is now FPGA Client Driver (FCD).
  - Runtime functions renamed from `clXXXXXXAltera` to `clXXXXXXIntelFPGA`.
  - Renamed channel functions as follows:
    - Renamed `read_channel_altera` to `read_channel_intel`.
    - Renamed `write_channel_altera` to `write_channel_intel`.
    - Renamed `read_channel_nb_altera` to `read_channel_nb_intel`.
    - Renamed `write_channel_nb_altera` to `write_channel_nb_intel`.

    You can continue to use the deprecated channel functions by specifying the `-D__IHC_USE_DEPRECATED_NAMES` parameter of the `aoc` command, or by adding the `#define __IHC_USE_DEPRECATED_NAMES` macro to the top of your kernel file.
  - Renamed platform related expressions as follows:
    - Renamed Platform Suffix from `Altera` to `IntelFPGA`
    - Renamed Vendor Name from `Altera Corporation` to `Intel Corporation`
    - Renamed SDK Name from `Altera OpenCL SDK` to `Intel(R) FPGA SDK for OpenCL(TM)`

1.2 Operating System Support

Information about OS support for the Intel FPGA SDK for OpenCL is available on the Operating System Support page of the Altera website.

Related Links

Operating System Support

1.3 Changes to Software Behavior

Items listed in the following table represent cases in which the behaviors of the current release of the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL differ from the previous version.

Description	Workaround
N/A	N/A

Items listed in the following table represent cases in which the behaviors of the current release of the Intel FPGA SDK for OpenCL Custom Platform Toolkit and Reference Platforms differ from the previous version.

Description	Workaround
N/A	N/A

1.4 Known Issues and Workarounds

This section provides information about known issues that affect the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 17.0.

Description	Workaround
N/A	N/A

This section provides information about known issues that affect the current release of the Intel FPGA SDK for OpenCL Custom Platform Toolkit and Reference Platforms. These issues might also affect Custom Platforms you create for use with the Intel FPGA SDK for OpenCL.

Description	Workaround
N/A	N/A

For additional known issue information for the current Intel FPGA SDK for OpenCL version, refer to the Knowledge Base web page.
Additional Known Software Issues Affecting the Intel FPGA SDK for OpenCL Version 17.0

Latest Known Intel FPGA SDK for OpenCL Software Issues

You can find known issue information for previous Intel FPGA SDK for OpenCL versions on the Knowledge Base web page.

Related Links

Knowledge Base

1.5 Software Issues Resolved

The following issues were corrected or otherwise resolved in the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 17.0.

Table 1. Issues Resolved in the Intel FPGA SDK for OpenCL and the Intel FPGA RTE for OpenCL Version 17.0

Customer Service Request Numbers		
11226385	11260485	112646607
11272585	11277099	11280203
11289468	11303447	11305424

1.6 Software Patches Included in this Release

Table 2. Software Patches Included in the Intel FPGA SDK for OpenCL Version 17.0

Software Version	Patch	Customer Service Request Number
Altera SDK for OpenCL version 16.0.1	2.02cl	11286111
Altera SDK for OpenCL version 16.0.1	2.01cl	-
Altera SDK for OpenCL version 16.0	0.03cl	-

1.7 Document Revision History

Table 3. Intel FPGA SDK for OpenCL Version 17.0 Release Notes Document Revision History

Date	Document Version	Changes
May 2017	2017.05.05	• Revised New Features and Enhancements on page 3 to reflect updates and enhancements made for Version 17.0. • Revised Software Issues Resolved on page 5 to reflect software issues resolved with Version 17.0. • Revised Software Patches Included in this Release on page 5 to reflect patches included with Version 17.0.
November 2016	2016.11.07	• Renamed document to *Intel FPGA SDK for OpenCL Release Notes* • Included the following new features and enhancements: — Rebranded names for the SDK, RTE, and compiler — Windows 10 support — SVM support — Image array support — Arria 10-specific single-cycle floating-point accumulator for single work-item kernels — Advanced features for enhanced design configuration — ACD Support for installing multiple Custom Platforms — Bit manipulation optimization in the offline compiler — `env` SDK utility option — `-g0` offline compiler command option — Arria® 10 GX FPGA Development Kit Reference Platform as part of the SDK installation — **Split read/write bursts on burst word boundary** parameter for the OpenCL Memory Bank Divider Qsys component in the Custom Platform Toolkit — HTML report (beta feature) • For SDK users: — 64-bit big-endian support is deprecated and removed — `analyze-area` SDK utility option is deprecated — Function of the `-g` offline compiler command option is now part of the offline compiler's default behavior — Kernel and IP source code is now embedded in the `.aocx` file — You must update your host code to instruct the `findPlatform()` function to search for "Intel(R) FPGA SDK for OpenCL", "Intel(R) FPGA SDK", or "Intel(R) FPGA", instead of "Altera", "Altera SDK", or other similar strings — If you compile a kernel with both the `--profile` and the `-g0` `aoc` command options, the source code of the kernel and IP will appear in the `.aocx` file — ACD and ICD are required when using Microsoft Visual Studio 2015 — You might encounter an `ip-generate FAILED` error, and a `qsys-archive: command not found` in the `.log` file when you compile an Arria 10 design • For board developers: — You need enable the **Split read/write bursts on burst word boundary** parameter in the OpenCL Memory Bank Divider Qsys component — Native Arria 10 GX FPGA Development kit must be configured by a field appplications engineer or a regional support center representative before use with the SDK

continued...

Date	Document Version	Changes
May 2016	2016.05.02	• Included the following new features and enhancements: — OpenCL pipes — Thread-safe host runtime environment — `#pragma ivdep` — Support for multi-device emulation — OpenCL library — Enhanced optimization reports • Included the following beta features and enhancements: — SVM support — Image array support — Enhanced area report — Arria 10-specific single-cycle floating-point accumulator for single work-item kernels — Advanced features for enhanced design configuration: • Kernel attributes for configuring on-chip local memory • Kernel attributes for reducing hardware overhead for single work-item kernels • Automatic kernel replication — Altera® Arria 10 GX FPGA Development Kit Reference Platform For AOCL users: • Noted that the AOC no longer creates a kernel-specific `.area` file that users can access. • For board developers, noted that the implementation of the AOCL `program` utility has changed. • Noted that designs targeting Arria 10 devices take longer to compile. For board developers: • Noted that in the `board_spec.xml` file, the `qsys_file` attribute now accepts the value `none`. • Advised that porting the Arria 10 GX FPGA Development Kit Reference Platform to use JTAG full-chip programming if PR does not function as expected. • Noted that the Forward Compatibility flow necessary for porting the Arria 10 GX FPGA Development Kit Reference Platform increases compilation time. The Forward Compatibility flow might also fail.
November 2015	2015.11.02	• Included the following production features and enhancements: — Windows 8.1 support. — Additional double precision floating-point functions. — `--high-effort` AOC command option. — Support for ICD and ACD. — Sub-buffers support. — `aoc` command without any argument. • Included the following beta features and enhancements: OpenCL pipes support, thread-safe host, image arrays support, and SVM support. • Included OpenCL Library as an early access feature. • Noted that there is a 64 kB lower limit on global memory allocation imposed by the runtime. • Noted that the AOCL is only downloadable as a tar file that also includes the Quartus® Prime software and device support. • Noted that you must set the *QUARTUS_ROOTDIR_OVERRIDE* environment variable to point to the correction edition of the Quartus Prime software. • Added emulation to the recommended setup flow for the AOCL. • Noted that OpenCL design examples no longer provide precompiled `.aocx` files. • Noted that the Emulator now supports kernels that implement pipes, including kernels that pass pipes and kernels by reference.

continued...

Date	Document Version	Changes
		• Noted that the `board_env.xml` file a Custom Platform must include the `mmdlib` XML element. • Noted that the AOCL `diagnose` utility must now support three internal calling modes. • Noted that installing unsigned drivers for AOCL running on Windows 8.1 might result in an error. • Noted that a license is not necessary to run the Altera RTE for OpenCL.
May 2015	15.0.0	• Included support for double precision floating-point functions as a new feature and listed the OpenCL-conformant functions. • Included the following beta features: — Implementation of OpenCL pipes — `--high-effort` Altera Offline Compiler (AOC) command option — OpenCL Installable Client Driver (ICD) extension support — Altera Client Driver (ACD) • Noted that naming a kernel source file kernel.cl causes a compilation error. • Noted that emulation of an OpenCL kernel design targeting an SoC must be performed on a non-SoC board. • Noted automigration is a change in software behavior starting in 14.1. • Noted that declaring a `__constant` pointer kernel argument in a kernel targeting a Cyclone V device might degrade kernel performance. • Noted the following Profiler limitations: — Do not include spaces in directory and file names. — Do not use the same kernel names across different `.aocx` files. — Adjusting the magnification of the **Kernel Executaion** tab might cause subtle changes to the time scale. • Noted that for Linux Power systems, the `init_opencl.sh` script now sets the correct paths for the *LD_LIBRARY_PATH* environment variable. • Noted that a third-party OpenCL SDK kernel with pipes implementation must be modified before running on the AOCL. • Noted that if a kernel with pipes implementation is
December 2014	14.1.0	• Included the following new features: — Single OpenCL license. — AOCL `uninstall` utility. — Hard floating-point support. — An *ALTERAOCLSDKROOT*`/init_opencl` script for setting environment variables transiently. — Custom Platform automigration as a beta functionality. • Noted that RHEL version 5.x is no longer supported. • Noted that a routing error might be solved by reducing kernel size. • Added notice the AOCL `program` and `diagnose` utilities now support the Cyclone V SoC Development Kit (c5soc). • Noted that emulation is not available to kernels targeting c5soc. • Noted that the end of an NDRange kernel cannot include a memory barrier. • Noted the erroneous *LD_LIBRARY_PATH* settings in the *ALTERAOCLSDKROOT*`/init_opencl.sh` script for big-endian systems. • Added notice that improper installation of the PLDA QuickUDP IP license might result in an error message that refers to the QuickTCP IP. • Added change notice for the command you run to verify that CMA is enabled successfully for c5soc. • Noted that the AOC might generate incorrect hardware for kernels targeting a board with only one bank of memory. • Noted that the `--util` <*N*> and `-O3` AOC options are deprecated. • Noted that the `board_spec.xml` file now includes a `compile` XML element.

continued...

Date	Document Version	Changes
		• Added notice of updated specifications for the `version` XML attributes in the `board_env.xml` and `board_spec.xml` files. • Added notice about new enum value arguments for the `aocl_mmd_get_offline_info` MMD API call. • Added notice about board partition in the c5soc Reference Platform. • Added notice that you no longer need to remove the `libstdc++` library files from the *ALTERAOCLSDKROOT*`/host/linux64/lib` directory.
June 2014	14.0.0	• Included Cyclone V SoC support and big-endian architecture support as new features. • Included the following new features: RTE, AOCL channels extension, optimization report for single work-item kernels, and AOCL Custom Platform. • Included emulator and profiler as new beta features. • Included RPM installation option for AOCL and RTE. • Added notice that `float3` argument types are supported in 14.0. • Added notice that kernel clock reconfiguration issue during `.aocx` file generation is fixed in 14.0. • Added notice that the issue with excessive memory consumption during full compilation is fixed in 14.0. • Added deprecation notices for the `--estimate-throughput` and `--sw-dimm-partition` AOC options. • Added deprecation notices for the `num_share_resources`, `max_share_resources`, `max_unroll_loop` and `task` kernel attributes. • Updated Linux version support. • Added support notice for OpenCL C++ bindings. • Added notice that, for Windows systems, trailing slashes in include paths are illegal. • Added notice that, for Windows systems, compilation fails if the file path to the kernel source file exceeds 260 characters in length. • Added notice that to disable burst-interleaving for the default global memory, `--no-interleaving` requires a default argument. • Added notice that AOC options for floating-point operations have been renamed (that is, `--fp-relaxed` and `--fpc`). • Added notice that the `program` and `flash` AOCL utilities require a device name argument. • Added notice that `aocl diagnostic` has been renamed to `aocl diagnose`. Invoking `aocl diagnose` queries a list of devices. Invoking `aocl diagnose` <*device_name*> runs board vendor's diagnostic tests on a specific board. • Added notices of Cyclone V SoC-specific AOCL limitations. • Added notice to exclude the `num_compute_units` kernel attribute in OpenCL kernel programs targeting big-endian systems. • Added notices of the *Altera SDK for OpenCL Optimization Guide* and the APBPP board package have been renamed.
December 2013	13.1.1	• Included multiple devices support as a new beta feature. • Included heterogeneous memory system as a new beta feature. • Included the `--no-interleaving` <*memory_type*> option of the aoc command. • Included new `buffer_location` kernel attribute. • Added notice to modify the contents of `$ALTERAOCLSDKROOT/host/linux64/lib` to remove OpenCL runtime incompatibility with C++ code compiled with GCC versions 4.3 and later.

continued...

Date	Document Version	Changes
November 2013	13.1.0	• Included the `--estimate-throughput` option of the aoc command. • Included new `task` kernel attribute. • Included restrictions on OpenCL filenames. • Updated installation and uninstallation instructions. • Updated location where OpenCL example applications can be downloaded. • Updated the name of the folder or directory to which the installer extracts the AOCL. • Updated setting of the *PATH* environment variable. • Updated setting to *LD_LIBRARY_PATH* environment variable. • Updated output of the `--report` flag of the aoc command. • Updated the AOCL support status for BittWare FPGA boards. • Updated the AOCL support status for kernel parameters. • Updated support status for `float3` argument types. • Included notice on premature termination of host application debugging process in GDB. • Included notice to modify `top.qsf` to avoid large memory consumption during full compilation.
June 2013	13.0 SP1.0	• Included new kernel attributes and new design example. • Updated *LM_LICENSE_FILE* setting for Windows and Linux systems. • Updated board driver installation instructions. • Updated the SDK installation instructions for Linux systems without preexisting `.cshrc` or `.bashrc` files. • Updated the locations of the board drivers for Nallatech and Bittware boards. • Updated the implementation status of the AOCL utility for the BittWare board. • Updated vendor and device IDs on Windows systems. • Updated path to design examples. • Updated path to the moving_average design example. • Updated flash programming instructions. • Updated file type support for `.aocx` files. • Updated support status of complex exit paths in kernel source code. • Added notices on figure updates in the *Altera SDK for OpenCL Optimization Guide*.
May 2013	13.0.0	• Initial Release.