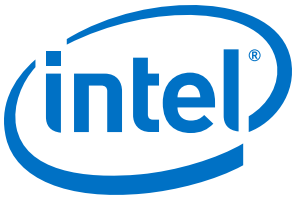

Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs 1.1 Release Notes

Updated for Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs: **1.1 Production**

RN-1209 | 2018.08.06
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Notice

Please note that the Intel® Acceleration Stack for Intel Xeon® CPU with FPGAs DOES NOT include mitigations for the exploits known as Spectre (CVE-2017-5753, CVE-2017-5715) and Meltdown (CVE-2017-5754). These exploits require that malware runs locally on the system, which is not normally possible in a closed environment where the system's software is centrally controlled. Intel does not recommend that an un-mitigated version of the Intel Acceleration Stack for Intel Xeon CPU with FPGAs be used in an environment that is not a closed system environment.

Intel Acceleration Stack for Intel Xeon CPU with FPGAs 1.1 Release Notes

This document provides up-to-date information about the Intel Acceleration Stack for Intel Xeon CPU with FPGAs 1.1 Production release.

Acceleration Acronym List

Use the following table as a reference when reviewing the release notes.

Table 1. Acronyms

Acronyms	Expansion	Description
AFU	Accelerator Functional Unit	Hardware Accelerator implemented in FPGA logic which offloads a computational operation for an application from the CPU to improve performance.
AF	Accelerator Function	Compiled Hardware Accelerator image implemented in FPGA logic that accelerates an application. An AFU and associated AFs may also be referred to as GBS (Green-Bits, Green BitStream) in the Acceleration Stack installation directory tree and in source code comments.
ASE	AFU Simulation Environment	Co-simulation environment that allows you to use the same host application and AF in a simulation environment. ASE is part of the Intel Acceleration Stack for FPGAs.
FIM	FPGA Interface Manager	The FPGA hardware containing the FPGA Interface Unit (FIU) and external interfaces for memory, networking, etc. The FIM may also be referred to as BBS (Blue-Bits, Blue BitStream) in the Acceleration Stack installation directory tree and in source code comments. The Accelerator Function (AF) interfaces with the FIM at run time.
HSSI	High-speed Serial Interface	Reference to the multi-gigabit serial transceiver I/O in the FIM and the corresponding interface to the Accelerator Functional Unit (AFU).

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Acronyms	Expansion	Description
OPAE	Open Programmable Acceleration Engine	The OPAE is a software framework for managing and accessing AFs.
PIM	Platform Interface Manager	An abstraction layer for managing top-level device ports and system-provided clock crossing.
PR	Partial Reconfiguration	The ability to dynamically reconfigure a portion of an FPGA while the remaining FPGA design continues to function.

Minimum Requirements

The minimum requirements for the Intel Programmable Acceleration Card with Intel Arria® 10 GX FPGA must include:

- Intel Xeon Scalable processor
- A PCI Express* x16 Slot
- 48 GB of free memory is a requirement only if you are compiling a hardware design
- Red Hat* Enterprise Linux* (RHEL) 7.4 or CentOS 7.4

Intel Acceleration Stack 1.1 Reference Table

Table 2. Intel Acceleration Stack 1.1 Reference Table

Intel Acceleration Stack Version	Platform	FPGA Interface Manager (FIM) Version: Partial Reconfiguration (PR) Interface ID	Open Programmable Acceleration Engine (OPAE) Version	Intel Quartus® Prime Pro Edition
1.1 Production(1)	Intel PAC with Intel Arria 10 GX FPGA	9926ab6d-6c92-5a68-aabc-a7d84c545738	1.0.2	17.1.1
1.1 Beta	Intel PAC with Intel Arria 10 GX FPGA	0f17997f-199b-5f75-9713-2653d3ce0176	1.0.1	17.1.1
1.1 Alpha	Intel PAC with Intel Arria 10 GX FPGA	8fd6574f-8f82-5164-9336-69c4bdaba437	0.14.0	17.1.1
1.0 Production(1)	Intel PAC with Intel Arria 10 GX FPGA	ce489693-98f0-5f33-946d-560708be108a	0.13.1	17.0.0

(1) When the image in the user partition cannot be loaded, a flash failover occurs and the factory image is loaded instead. After a flash failover occurs, the PR ID reads as d4a76277-07da-528d-b623-8b9301feaffe.

Enhancements

Table 3. 1.0 Production to 1.1 Production Enhancements in the Intel Acceleration Stack Version

Note: No enhancements were introduced from 1.1 Beta to 1.1 Production.

Area	Enhancement
Intel Quartus Prime Pro Edition	Supports version 17.1.1
Accelerator Functional Unit (AFU)	Support for 10 Gbps and 40 Gbps Ethernet MAC • Introduces HSSI interface to Accelerator Functional Unit (AFU) • Introduces 4x10G and 40G AFU examples that use HSSI interface
FPGA Interface Manager (FIM)	• Floorplan changes to accommodate larger OpenCL* designs. • Timing and performance improvements to OpenCL • Increase of memory-mapped I/O (MMIO) timeout
OPAE	Addition of Platform Interface Manager (PIM)
DMA	• New streaming DMA AFU. • Optimized DMA memory-mapped AFU driver code to improve bandwidth.
HSSI	• Added OPAE C applications for the 10 Gbps and 40 Gbps Ethernet MAC AFU examples. • Added commands to `pac_hssi_config.py`: `eqwrite`, `eqread` and `eeprom`. • Added HSSI tuning capability to `pac_hss_config.py`. • Added driver support for HSSI. • Updated HSSI DEV_FEATURE_HDR (DFH) ID to 0x0A.
OpenCL	• Updated OpenCL error handling to prevent spurious error messages. • Added environment variables to enable non-uniform memory architecture (NUMA) awareness and thread binding for DMA performance. • Multi-card support for aocl diagnose.
`fpgainfo` Tool	Updated to display human readable FIM IDs that follow Acceleration Stack version numbering.
Native Loopback (NLB) AFU	Added pCLK frequency information to a control and status register (CSR).
Platform Interface Manager (PIM)	Updated the mechanism for finding the PIM platform class and database.

Known Issues

Table 4. Known Issues for the Intel Acceleration Stack 1.1 Production Version

Known Issue	Details
PCIe directed speed changes are not supported.	Only automatic down-training at boot time is supported.
Invalid memory read fault may cause FIM to lock.	• The FIM locks after the AFU sends a memory read to invalid address. • Workaround: Power cycle the system to reinitialize the Intel PAC with Intel Arria 10 GX FPGA and recover from this issue. Refer to the Knowledge Base entry for more information. • Status: Fix targeted for a future version of the Intel Acceleration Stack.
	continued...

Known Issue	Details
Designs may not function properly when a customer loads a second AFU.	• Designs may not function properly when a customer loads an AFU for a second time using fpgaconf. • Workaround: Power cycle the system to reinitialize the Intel PAC with Intel Arria 10 GX FPGA so that you can use fpgaconf to load another AFU. For more information, refer to the *Identifying and Updating the FIM* section of the *Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA*. • Status: Fix targeted for a future version of the Intel Acceleration Stack.
Streaming DMA only supports access to host memory.	• The streaming DMA basic buidling blocks (BBBs) can access host or FPGA memory, but the driver does not provide any means for accessing FPGA memory. • Status: This limitation will be fixed in a future version of the driver.
Memory-to-stream DMA does not assert start-of-packet (SOP) at the beginning of a packet transfer.	• The memory-to-stream DMA supports packet transfers but it currently does not assert start-of-packet (SOP) at the beginning of a packet transfer. • Status: This limitation will be fixed in a future version of the driver.
Length argument to the driver is ignored when performing a non-deterministic length stream-to-memory transfer.	• When performing a non-deterministic length stream-to-memory transfer, the length argument to the driver is ignored. • Workaround: To prevent the DMA from overflowing, the host buffer ensures that it is sufficiently sized so that the stream-to-memory DMA receives an end-of-packet (EOP) before overflowing the host buffer. • Status: This limitation will be fixed in a future version of streaming DMA.
Virtual Function (VF) may fail to attach or detach when using the Linux Red Hat* 3.10 kernel.	The VF failure to attach or detach is a known issue with `qemu/kvm` and `libvirt`. Refer to the Red Hat website for more information about this issue.

Related Information

Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA

Resolved Issues

Table 5. Issues Resolved from 1.1 Beta to 1.1 Production in the Intel Acceleration Stack Software

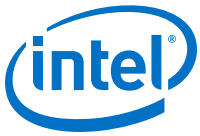
Area	Description
Quad Small Form-factor Pluggable (QSFP) cables.	If you hot swap QSFP cables, the sensors are now able to read temperature and voltage accurately. You must update the BMC firmware to version 26822 to inherit this fix. Refer to the *Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA* for steps on how to update the firmware.
Part Numbering in the Intel Quartus Prime Pro Edition design example.	The Intel Quartus Prime Pro Edition design example now uses the correct Intel PAC with Intel Arria 10 GX FPGA part number: 10AX115N2F40E2LG.

Table 6. Issues Resolved from 1.0 Production to 1.1 Production in the Intel Acceleration Stack Software

Area	Description
The Intel FPGA Dynamic Profiler Tool for OpenCL	The graphical user interface (GUI) of the tool now reports correct frequency and bandwidth.
fpgainfo and fpgabist Tool	The fpgainfo tool no longer raises a `UnicodeEncodeError` when the Python* interpreter cannot determine what encoding to use. This issue typically occurred when redirecting or piping output on previous versions of the Intel Acceleration Stack. The fpgabist was also impacted.
AFU Sample Code	You can now read valid values from `af2cp_sTxPort.c1.hdr.rsvd2[5:4]` when simulating the `hello_intr_afu` sample code.

Related Information

Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA



Intel Acceleration Stack for Intel Xeon CPU with FPGAs 1.1 Release Notes Revision History

Date	Acceleration Stack Version	Changes
2018.08.06	1.1 Production (compatible with Intel Quartus Prime Pro Edition 17.1.1)	• Noted new enhancements, known issues and resolved issues from 1.0 Production to 1.1 Production. • Noted new enhancements, known issues and resolved issues since 1.1 Beta release.
2018.05.29	1.1 Beta (compatible with Intel Quartus Prime Pro Edition 17.1.1)	Noted new enhancements, known issues and resolved issues since the 1.1 Alpha release.
2018.04.16	1.1 Alpha (compatible with Intel Quartus Prime Pro Edition 17.1.1)	Initial release