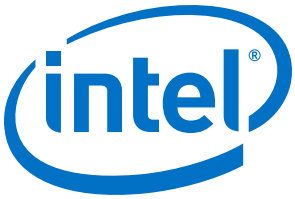

Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs Release Notes

Updated for Intel® Acceleration Stack: **1.0 Production**

RN-1207 | 2018.04.11
Latest document on the web: PDF | HTML

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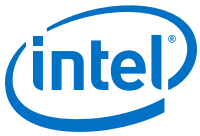


Notice

Please note that the Intel® Acceleration Stack for Intel Xeon® CPU with FPGAs DOES NOT include mitigations for the exploits known as Spectre (CVE-2017-5753, CVE-2017-5715) and Meltdown (CVE-2017-5754). These exploits require that malware runs locally on the system, which is not normally possible in a closed environment where the system's software is centrally controlled. Intel does not recommend that an un-mitigated version of the Intel Acceleration Stack for Intel Xeon CPU with FPGAs be used in an environment that is not a closed system environment.

Intel Acceleration Stack for Intel Xeon CPU with FPGAs Release Notes

This document provides up-to-date information about the Intel Acceleration Stack for Intel Xeon CPU with FPGAs 1.0 Production release.

Acceleration Acronym List

Use the following table as a reference when reviewing the release notes.

Table 1. Acronyms

Acronyms	Expansion	Description
AFU	Accelerator Functional Unit	Hardware Accelerator implemented in FPGA logic which offloads a computational operation for an application from the CPU to improve performance.
AF	Accelerator Function	Compiled Hardware Accelerator image implemented in FPGA logic that accelerates an application. An AFU and associated AFs may also be referred to as GBS (Green-Bits, Green BitStream) in the Acceleration Stack installation directory tree and in source code comments.
ASE	AFU Simulation Environment	Co-simulation environment that allows you to use the same host application and AF in a simulation environment. ASE is part of the Intel Acceleration Stack for FPGAs.
FIM	FPGA Interface Manager	The FPGA hardware containing the FPGA Interface Unit (FIU) and external interfaces for memory, networking, etc. The FIM may also be referred to as BBS (Blue-Bits, Blue BitStream) in the Acceleration Stack installation directory tree and in source code comments. The Accelerator Function (AF) interfaces with the FIM at run time.
OPAE	Open Programmable Acceleration Engine	The OPAE is a software framework for managing and accessing AFs.
PR	Partial Reconfiguration	The ability to dynamically reconfigure a portion of an FPGA while the remaining FPGA design continues to function.

System Requirements

The following servers have been tested for this release:

- Dell* R640
- Dell R740

The best known server configuration with the Intel Programmable Acceleration Card with Intel Arria® 10 GX FPGA must include:

- Intel Xeon Scalable processor
- A PCI Express* x16 Slot
- RAM: 48 GB
- Red Hat* Enterprise Linux* (RHEL) 7.4 or CentOS 7.4

Intel Acceleration Stack 1.0 Reference Table

Table 2. Intel Acceleration Stack 1.0 Reference Table

Intel Acceleration Stack Version	Platform	FPGA Interface Manager (FIM) Version (Partial Reconfiguration (PR) Interface ID)	Open Programmable Acceleration Engine (OPAE) Version	Intel Quartus® Prime Pro Edition
1.0 Production(1)	Intel PAC with Intel Arria 10 GX FPGA	ce489693-98f0-5f33-946d-560708be108a	0.13.1	17.0.0

Enhancements

Table 3. Enhancements in the Intel Acceleration Stack Version 1.0

Area	Enhancement
FPGA Interface Manager (FIM)	Improved floor plan and included partial reconfiguration (PR) timing constraints to provide more resources for accelerator functions (AFs).

Known Issues

Table 4. Known Issues for the Intel Acceleration Stack 1.0 Production

Known Issue	Details
A different OPN is used in the design examples.	The Intel Quartus Prime Pro Edition license uses a design example OPN of 10AX115N3F40E2SG, instead of the Intel PAC with Intel Arria 10 GX FPGA OPN of 10AX115N2F40E2LG. This difference does not impact your design. The design example OPN variance will be corrected to match the platform OPN in the Intel Acceleration Stack 1.1 version.
PCIe directed speed changes are not supported.	Only automatic down-training at boot time is supported.

continued...

(1) The factory partition of the configuration flash contains the Acceleration Stack 1.0 Alpha version. When the image in the user partition cannot be loaded, a flash failover occurs and the factory image is loaded instead. After a flash failover occurs, the PR ID reads as d4a76277-07da-528d-b623-8b9301feaffe.

Known Issue	Details
Virtual Function (VF) may fail to attach or detach when using the Linux Red Hat* 3.10 kernel. This is a known issue with `qemu/kvm` and `libvirt`.	Refer to the Red Hat* website for more information about this issue.
The Intel FPGA Dynamic Profiler Tool for OpenCL* GUI reports frequency and bandwidth incorrectly.	This issue will be resolved in a future version of Intel Acceleration Stack.

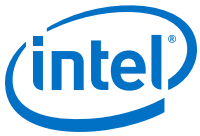
fpgainfo may raise a `UnicodeEncodeError` when the Python* interpreter cannot determine what encoding to use. This issue typically occurs when redirecting or piping output. The fpgabist tool calls fpgainfo and is also impacted.	There are two workarounds for this issue:
	• Set the `PYTHONENCODING` environment variable to UTF-8.
	• Modify the fpgainfo script to force the use of UTF-8:
	— Add an `import codecs` statement at the top of the file with the other import statements.
	— Before the line that calls `args.func(args)`, insert this comment and code line:
	`# wrap stdout with the StreamWriter that does unicode`
	`sys.stdout = codecs.getwriter('UTF-8')(sys.stdout)`

When simulating the `hello_intr_afu` sample code, the `af2cp_sTxPort.c1.hdr.rsvd2[5:4]` has a value of X.	This issue will be resolved in the Intel Acceleration Stack 1.1 version.

Issues Resolved

Table 5. Issues Resolved in the Intel Acceleration Stack Version 1.0

Area	Description
fpgabist Tool and DMA	Bandwidth numbers reported by dma_test are now accurate.
FPGA Interface Manager (FIM)	When using the automatic virtual channel (VA), all AFU traffic now routes to VH0 (PCIe). The routing assignment was undefined in the Acceleration Stack 1.0 Beta release.
Open Programmable Acceleration Engine (OPAE)	OpenCL host applications now handle all kernel interrupts. In the Acceleration Stack 1.0 Beta version, the host application may hang due to missing kernel interrupts.
Accelerator Functional Unit (AFU)	`run.sh` no longer requires two SR-IOV licenses when using a floating license. The Acceleration Stack 1.0 Beta version requests two licenses in this case.



Intel Acceleration Stack for Intel Xeon CPU with FPGAs Release Notes Revision History

Date	Acceleration Stack Version	Changes
2018.04.11	1.0 Production (compatible with Intel Quartus Prime Pro Edition 17.0.0)	Initial release.