Intel® High Level Synthesis Compiler Pro Edition

Version 20.3 Release Notes

Updated for Intel® Quartus® Prime Design Suite: **20.3**

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1. Intel® High Level Synthesis Compiler Pro Edition Version 20.3 Release Notes

The *Intel® High Level Synthesis Compiler Pro Edition Release Notes* provide late-breaking information about the Intel High Level Synthesis Compiler Pro Edition Version 20.3.

For the most recent Standard Edition release notes, see the Intel High Level Synthesis Compiler Standard Edition Release Notes.

About the Intel HLS Compiler Pro Edition Documentation Library

Documentation for the Intel HLS Compiler Pro Edition is split across a few publications. Use the following table to find the publication that contains the Intel HLS Compiler Pro Edition information that you are looking for:

Table 1. Intel High Level Synthesis Compiler Pro Edition Documentation Library

Title and Description	PRO
Release Notes Provide late-breaking information about the Intel HLS Compiler.	Link
Getting Started Guide Get up and running with the Intel HLS Compiler by learning how to initialize your compiler environment and reviewing the various design examples and tutorials provided with the Intel HLS Compiler.	Link
User Guide Provides instructions on synthesizing, verifying, and simulating intellectual property (IP) that you design for Intel FPGA products. Go through the entire development flow of your component from creating your component and testbench up to integrating your component IP into a larger system with the Intel Quartus Prime software.	Link
Reference Manual Provides reference information about the features supported by the Intel HLS Compiler. Find details on Intel HLS Compiler command options, header files, pragmas, attributes, macros, declarations, arguments, and template libraries.	Link
Best Practices Guide Provides techniques and practices that you can apply to improve the FPGA area utilization and performance of your HLS component. Typically, you apply these best practices after you verify the functional correctness of your component.	Link
Quick Reference Provides a brief summary of Intel HLS Compiler declarations and attributes on a single two-sided page.	Link

1.1. New Features and Enhancements

The Intel High Level Synthesis Compiler Pro Edition Version 20.3 includes the following new features:

- Added a new Loop Viewer to the High-Level Design Reports. The Loop Viewer provides a visualization of the behavior of loops in your designs.
- Enhanced the Loop Analysis Report (part of the High-Level Design Reports) with a new pane that shows information about loop bottlenecks.
- Enhanced the function of HLS pipes (`ihc::pipe`) so that you can now use pipes as interfaces from your component to its testbench.
- Enhanced loop fusion to support fusing loops with different trip counts. In previous compiler versions, only loops with the same trip count would be considered for fusing.

  The Intel HLS Compiler only considers adjacent loops with same trip count for automatic loop fusion. Use the `loop_fuse` pragma to tell the compiler to consider adjacent loops with different trip counts for fusing.

1.2. Changes in Software Behavior

The section documents instances where Intel HLS Compiler Pro Edition Version 20.3 features have changed from earlier releases of the compiler.

- The `--fpc` i++ command option was removed. Use the `-ffp-contract=fast` command option instead.
- The `--fp-relaxed` i++ command option was removed. Use the `-ffp-reassoc` command option instead.
- The Intel HLS Compiler now exits and returns an error message when it detects an irreducible loop. Previously, the compiler would exit without an error message.
- The limitation on the maximum size of dividers for AC data types has changed:
  - For `ac_int` data types, dividers are limited to a maximum of 128 bits unsigned or 127 bits signed.
  - For `ac_fixed` data types, dividers are limited to a maximum of 64 bits (unsigned or signed).

  In previous releases, the dividers for all AC data types were limited to consuming a maximum of 64 bits.
- (Windows only) Library functions that use HLS systems of tasks can now be emulated. Previously, emulating library functions that use systems of tasks was available only on Linux operating systems.
- The f_{MAX} II report is removed from the High-Level Design Reports. Its content is available in the Loop Analysis report.
- Support for Windows Server* 2016 is added.
- Support for Red Hat* Enterprise Linux* Server 6 is removed.

1.3. Intel High Level Synthesis Compiler Pro Edition Prerequisites

The Intel HLS Compiler Pro Edition is part of the Intel Quartus® Prime Pro Edition Design Suite. You can install the Intel HLS Compiler as part of your Intel Quartus Prime software installation or install it separately. It requires Intel Quartus Prime and additional software to use.

For detailed instructions about installing Intel Quartus Prime Pro Edition software, including system requirements, prerequisites, and licensing requirements, see Intel FPGA Software Installation and Licensing.

The Intel HLS Compiler requires the following software in addition to Intel Quartus Prime:

C++ Compiler

On Linux, Intel HLS Compiler requires GCC 9.1.0 including the GNU C++ library and binary utilities (binutils).

This version of GCC is provided as part of your Intel HLS Compiler installation. After installing the Intel HLS Compiler, GCC 9.1.0 is available in `<quartus_installdir>/gcc`.

Important: The Intel HLS Compiler uses the `<quartus_installdir>/gcc` directory as its toolchain directory. Use this installation of GCC for all your HLS-related design work.

For Windows, install one of the following versions of Microsoft* Visual Studio* Professional:

- Microsoft Visual Studio 2017 Professional
- Microsoft Visual Studio 2017 Community

Important: The Intel HLS Compiler software does not support versions of Microsoft Visual Studio other than those specified for the edition of the software.

Mentor Graphics* ModelSim* Software

On Windows and RedHat Linux systems, you can install the ModelSim* software from the Intel Quartus Prime software installer. The available options are:

- ModelSim - Intel FPGA Edition
- ModelSim - Intel FPGA Starter Edition

Alternatively, you can use your own licensed version of Mentor Graphics* ModelSim or Mentor Graphics* Questa* Advanced Simulator software.

On Red Hat Linux systems, ModelSim software requires the Red Hat development tools packages. Additionally, any 32-bit versions of ModelSim software (including those provided with Intel Quartus Prime) require additional 32-bit libraries. The commands to install these requirements are provided in Installing the Intel HLS Compiler on Linux Systems.

On SUSE* Linux systems, you must use your own licensed version of Mentor Graphics ModelSim software.

For information about all the ModelSim software versions that the Intel software supports, refer to the *EDA Interface Information* section in the Software and Device Support Release Notes for your edition of Intel Quartus Prime Pro Edition

Related Information

- Intel High Level Synthesis Compiler Getting Started Guide
- Supported Operating Systems
- Software Requirements
  in *Intel FPGA Software Installation and Licensing*
- EDA Interface Information (Intel Quartus Prime Pro Edition)
- Mentor Graphics ModelSim Website

1.4. Known Issues and Workarounds

This section provides information about known issues that affect the Intel HLS Compiler Pro Edition Version 20.3.

Description	Workaround
(Windows only) Compiling a design in a directory with a long path name can result in compile failures.	Compile the design in a directory with a short path name.
(Windows only) A long path for your Intel Quartus Prime installation directory can prevent you from successfully compiling and running the Intel HLS Compiler tutorials and example designs.	Move the tutorials and examples to a short path name before trying to run them.
Libraries that target OpenCL* and are written in HLS cannot use streams or pipes as an interface between OpenCL code and the library written in HLS. However, the library in HLS can use streams or pipes if both endpoints are within the library (for example, a stream that connects two task functions).	N/A
Libraries that target OpenCL and are written in HLS might cause OpenCL kernels that include the library to have a more conservative incremental compilation.	N/A

When developing a library, if you have a `#define` defining a value that you use later in a `#pragma`, the `fpga_crossgen` command fails.
For example, the following code cannot be compiled by the `fpga_crossgen` command:
`#define unroll_factor 5`
 	
`int foo(int array_size) {`
`  int tmp[100];`
`  int sum =0;`
`//pragma unroll unroll_factor`
`#pragma ivdep array(tmp) safelen(unroll_factor)`
`  for (int i=0;i<array_size;i++) {`
`    sum+=tmp[i];`
`  }`
`  return sum;`
`}`
	Use `__pragma` instead of `#pragma`.
	For example, the following compiles successfully with the `fpga_crossgen` command:
	`#define unroll_factor 5`
	
	`int foo(int array_size) {`
	`  int tmp[100];`
	`  int sum =0;`
	`//pragma unroll unroll_factor`
	`__pragma ivdep array(tmp) safelen(unroll_factor)`
	`  for (int i=0;i<array_size;i++) {`
	`    sum+=tmp[i];`
	`  }`
	`  return sum;`
	`}`

When you use the `-c` command option to have separate compilation and linking stages in your workflow, and if you do not specify the `-march` option in the linking stage (or specify a different `-march` option value), your linking stage might fail with or without error messages.	Ensure that you use the same `-march` option value for both the compilation with the `-c` command option stage and the linking stage.

Applying the `hls_merge` memory attribute to an array declared within an unrolled or partially unrolled loop causes copies of the array to be merged across the unrolled loop iterations.
`#pragma unroll 2`
`for (int I = 0; I < 8; i++) {`
`   hls_merge(“WidthMerged”, “width”) int MyMem1[128];`
`   hls_merge(“WidthMerged”, “width”) int MyMem2[128];`
`   ...`
`   hls_merge(“DepthMerged”, “depth”) int MyMem3[128];`
`   hls_merge(“DepthMerged”, “depth”) int MyMem4[128];`
`   ...`
`}`
	Avoid using the `hls_merge` memory attribute in unrolled loops.
	If you need to merge memories in an unrolled loop, explicitly declare an array of struct type for width merging, or declare a deeper array for depth merging.
	`struct Type {int A; int B;};`
	`#pragma unroll 2`
	`for (int I = 0; I < 8; i++) {`
	`   Type WidthMerged[128];  // Manual width merging`
	`   ...`
	`   int DepthMerged[256];   // Manual depth merging`
	`   ...`
	`}`

In the Function Memory Viewer high-level design report, some function-scoped memories might appear as "optimized away".	None. When a file contains functions that are components and functions that are not components, all function-scoped variables are listed in the Function Memory List pane, but only variables from components have information about them to show in the Function Memory View pane.
Some high-level design reports fail in Microsoft Internet Explorer*.	Use one of the following browsers to view the reports:

continued...

Description	Workaround
	• Google Chrome* • Microsoft Edge* • Mozilla* Firefox*
The Loop Viewer in the High-Level Design Reports has the following restrictions: • The behavior of stall-free clusters is not modeled in the Loop Viewer. The final latency shown in the Loop Viewer for a stall-free cluster is typically more pessimistic (that is, higher) than the actual latency of your design. For a description of clustering and stall-free clusters, refer to *Clustering the Datapath* in the *Intel High Level Synthesis Compiler Pro Edition Best Practices Guide*. • Stalls from reads and writes from memory or print statements are not modeled. • High-iteration counts (>1000) cause slow performance of the Loop Viewer. • You cannot specify an iteration count of zero (0) in the Loop Viewer.	None.
Links in some reports in the High-Level Design Reports generated on Windows systems do not work.	Generate the High-Level Design Reports (that is, compile your code) on a Linux system.

Using a `struct` of a single `ac_int` data type in steaming interface that uses packets (`ihc::usesPackets<true>`) does not work.
For example, the following code snippet does not work:
`// class definition`
`class DataType {`
`      ac_int<155, false> data;`
`...`
`}`
`// stream definition`
`typedef ihc::stream_in<DataType,`
`                       ihc::usesPackets<true>,`
`                       ihc::usesEmpty<true>`
`                      > DataStreamIn;`
	To use this combination in your design, obey the following restrictions:
	• The internal `ac_int` data size must be multiple of 8
	• The stream interface type declaration must specify `ihc::bitsPerSymbol<8>`
	For example, the following code snippet works:
	`// class definition`
	`class DataType {`
	`      ac_int<160, false> data;`
	`// data width must be multiple of 8`
	`...`
	`}`
	`// stream definition`
	`typedef ihc::stream_in<DataType,`
	`                       ihc::usesPackets<true>,`
	`                       ihc::usesEmpty<true>,`
	`                       ihc::bitsPerSymbol<8>`
	`                      > DataStreamIn;`
	`// added ihc::bitsPerSymbol<8>`

When running a high-throughput simulation of your component using enqueue function calls, if you do not use the `ihc_hls_component_run_all` function to run the enqueued component calls after all of the `ihc_hls_enqueue` calls for that component, the following behaviors occur: • In emulation, the enqueued component functions are run. • In simulation, the enqueued component functions are not run, with no error or warning messages provided.	Ensure that you use the `ihc_hls_component_run_all` function after all of the `ihc_hls_enqueue` calls for that component to run enqueued component function calls.

Launching a task function with `ihc::launch_always_run` strips away optimization attributes applied to the task function.
In the following code example, the attribute applied to the function is ignored. The High-Level Design Reports show an II of 1 for this task instead of the requested II of 4.
`hls_component_ii(4) void noop()`
`{`
`    bool sop, eop;`
`    int empty;`
`    auto const data = data_in.read(sop, eop, empty);`
	To avoid stripping away the optimization, add a `while(1)` loop to the affected function apply the corresponding control pragma to the `while(1)` loop instead of the function.
	The following code example show how you can implement this change for the earlier code example:
	`void noop()`
	`{`
	`#pragma ii 4`
	`    while (1)`
	`    {`
	`        bool sop, eop;`
	`        int empty;`
	`        auto const data = data_in.read(sop, eop,`

continued...

Description	Workaround

data_out.write(data, sop, eop, empty);
}
 	
component void main_component()
{
    ihc::launch<noop>();
}
	empty);
	
	        data_out.write(data, sop, eop, empty);
	    }
	}
	
	component void
	main_component()
	{
	    ihc::launch_always_run<noop>();
	}

Only when simulating your component, the `startofpacket` signal of a stream interface might behave incorrectly in simulation in some rare situations that involve non-power-of-2 wide streams. Generated hardware does not have this issue.	If you encounter this issue, pad your stream to a power-of-two width for simulation.

1.5. Software Issues Resolved

The following issues were corrected or otherwise resolved in the Intel HLS Compiler Pro Edition Version 20.3.

Table 2. Issues Resolved in the Intel HLS Compiler Pro Edition Version 20.3

Customer Service Request Numbers						
00443282	00499721					

1.6. Intel High Level Synthesis Compiler Pro Edition Release Notes Archives

Intel HLS Compiler Version	Title
20.2	Intel High Level Synthesis Compiler Pro Edition Version 20.2 Release Notes
20.1	Intel High Level Synthesis Compiler Pro Edition Version 20.1 Release Notes
19.4	Intel High Level Synthesis Compiler Pro Edition Version 19.4 Release Notes
19.3	Intel High Level Synthesis Compiler Pro Edition Version 19.3 Release Notes
19.2	Intel High Level Synthesis Compiler Pro Edition Version 19.2 Release Notes
19.1	Intel High Level Synthesis Compiler Pro Edition Version 19.1 Release Notes
18.1	Intel High Level Synthesis Compiler Version 18.1 Release Notes
18.0	Intel High Level Synthesis Compiler Version 18.0 Release Notes
17.1	Intel High Level Synthesis Compiler Version 17.1 Release Notes

1.7. Document Revision History for Intel HLS Compiler Pro Edition Version 20.3 Release Notes

Document Version	Intel Quartus Prime Version	Changes
2020.09.28	20.3	• Initial release.