The Arria 10 system on a chip (SoC) hard processor system (HPS) release notes provides late-breaking information about the ACDS 13.1a10 software.

These release notes describe the following topics:

- Features supported by the Arria 10 SoC HPS
- Intellectual property (IP) for the Arria 10 SoC HPS, including the Arria 10 SoC HPS component
- Embedded software for the Arria 10 SoC HPS
- Known issues and Errata

Related Information
Quartus II Software and Device Support Release Notes

Product Revision History

Table 1: SoC HPS Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
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<tbody>
<tr>
<td>13.1a10</td>
<td>December 2013</td>
<td>Initial release</td>
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Features Supported by the SoC HPS

What to Expect in Arria 10 SoC HPS for v13.1 A10

The Arria 10 SoC HPS software v. 13.1a10 includes the following features:

- Simulation support or IP interfacing the HPS via Advanced eXtensible Interface (AXI™) bus functional model (BFM)
  - Clock and reset
  - FPGA-to-HPS ARM® Advanced Microcontroller Bus Architecture (AMBA®) AXI slave
  - HPS-to-FPGA AXI master
  - Lightweight HPS-to-FPGA AXI master
  - FPGA-to-HPS SDRAM AXI slave
  - Microprocessor unit (MPU) general-purpose I/O (GPIO)
  - MPU standby and event
  - Interrupts
  - Direct memory access (DMA) controller peripheral request
  - FPGA cross trigger
  - System Trace Macrocell (STM™) hardware event

- HPS MegaWizard support including:
  - FPGA interfaces
    - Peripheral pins multiplexing to FPGA fabric
  - HPS clocks and resets
    - Alternate clock source from FPGA
    - HPS-to-FPGA user0 clock
    - HPS-to-FPGA user1 clock
    - HPS warm reset handshake signals
    - HPS-to-FPGA cold reset output
    - FPGA-to-HPS debug reset request
    - FPGA-to-HPS warm reset request
    - FPGA-to-HPS cold reset request
    - Peripheral device clock output to FPGA interface multiplexing to FPGA fabric
      - Ethernet media access controller (EMAC)
      - Quad serial peripheral interface (QSPI)
      - Secure digital / multimedia card (SD/MMC)
      - SPI master
      - Inter-integrated circuit (I2C)
Interrupts
- FPGA-to-HPS
- HPS-to-FPGA
  - Clock peripheral
  - Cross trigger interface (CTI)
  - Direct memory access (DMA)
  - EMAC
  - FPGA manager
  - General purpose IP (GPIP)
  - Hard memory controller (HMC)
  - I²C
  - Level 4 (L4) timer
  - NAND
  - SYS timer
  - QSPI
  - SD/MMC
  - SPI master
  - SPI slave
  - Universal asynchronous receiver transmitter (UART)
  - Watchdog

FPGA EMAC switch interface
- EMAC0
- EMAC1
- EMAC2

Security manager
- Anti-tamper interface between the FPGA and the HPS security manager

DMA peripheral request
- Up to six request IDs

FPGA-to-HPS SDRAM interface
- AXI bridge with 32, 64, and 128 bits

HPS FPGA bridge
- FPGA-to-HPS
- HPS-to-FPGA
- Lightweight HPS-to-FPGA

MPU standby and event signal
MPU general purpose signal
- Debug advanced peripheral bus (APB™) interface
STM hardware events
- FPGA cross trigger interface
- FPGA trace port interface
- Boot from FPGA signals
- JTAG interface
Intellectual Property for the SoC HPS

For details of external memory interface soft IP supported by the Arria 10 SoC device, refer to the External Memory Interface Spec Estimator page at www.altera.com.

For details of other soft IP supported by the Arria 10 SoC device, refer to the Altera Product Selector page at www.altera.com.

Related Information

- External Memory Interface Spec Estimator
- Altera Product Selector

Known Issues and Errata

The following list identifies known issues and errata for the Arria 10 SoC HPS software v. 13.1a10:

- HPS MegaWizard does not currently support
  - HPS peripheral pin MUX GUI
    - HPS I/O multiplexing is not supported
  - HPS to SDRAM interface
    - Ready latency is not supported in 13.1a10

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