Intel® Stratix® 10

INTEL® STRATIX® 10 MX (DRAM SYSTEM-IN-PACKAGE) PRODUCT TABLE

	PRODUCT LINE	MX 1650	MX 1650	MX 1650	MX 2100	MX 2100	MX 2100	MX 2100
Resources	Logic elements (LEs)[1]	1,679,000	1,679,000	1,679,000	2,073,000	2,073,000	2,073,000	2,073,000
	Adaptive logic modules (ALMs)	569,200	569,200	569,200	702,720	702,720	702,720	702,720
	ALM registers	2,276,800	2,276,800	2,276,800	2,810,880	2,810,880	2,810,880	2,810,880
	Hyper-Registers from Intel® Hyperflex™ FPGA architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric						
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees						
	HBM2 high-bandwidth DRAM memory (GBytes)	8	16	8	8	8	16	8
	eSRAM memory blocks	2	2	2	2	2	2	2
	eSRAM memory size (Mb)	94.5	94.5	94.5	94.5	94.5	94.5	94.5
	M20K memory blocks	6,162	6,162	6,162	6,847	6,847	6,847	6,847
	M20K memory size (Mb)	120	120	120	134	134	134	134
	MLAB memory size (Mb)	9	9	9	11	11	11	11
	Variable-precision digital signal processing (DSP) blocks	3,326	3,326	3,326	3,960	3,960	3,960	3,960
	18 x 19 multipliers	6,652	6,652	6,652	7,920	7,920	7,920	7,920
	Peak fixed-point performance (TMACS)[2]	13.3	13.3	13.3	15.8	15.8	15.8	15.8
	Peak floating-point performance (TFLOPS)[3]	5.3	5.3	5.3	6.3	6.3	6.3	6.3
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitsream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection						
	Hard processor system[4]	–	–	–	–	–	–	–
	Maximum user I/O pins	656	656	584	640	656	656	584
	LVDS pairs 1.6 Gbps (RX or TX)	312	312	288	312	312	312	288
	Total full duplex transceiver count	96	96	96	48	96	96	96
	GXE transceiver count - PAM4 (up to 57.8 Gbps) or NRZ (up to 28.9 Gbps)	0	0	36 PAM-4 72 NRZ	0	0	0	36 PAM-4 72 NRZ
	GXT transceiver count - NRZ (up to 28.3 Gbps)	64	64	16	32	64	64	16
	GX transceiver count - NRZ (up to 17.4 Gbps)	32	32	8	16	32	32	8
	PCI Express* (PCIe*) hard intellectual property (IP) blocks (Gen3 x16)	4	4	1	2	4	4	1
	100G Ethernet MAC (no FEC) hard IP blocks	4	4	1	2	4	4	1
	100G Ethernet MAC + FEC hard IP blocks	0	0	12	0	0	0	12
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys						
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, E-Tile Transceiver Count and H-Tile Transceiver Count[5, 6]								
F2597 pin (52.5 mm x 52.5 mm, 1.0mm pitch)		656, 32, 312, 0, 96	656, 32, 312, 0, 96	–	640, 16, 312, 0, 48	656, 32, 312, 0, 96	656, 32, 312, 0, 96	–
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)		–	–	584, 8, 288, 72, 24	–	–	–	584, 8, 288, 72, 24

Notes:
1. LE counts valid in comparing across Altera devices, and are conservative vs. competing FPGAs.
2. Fixed point performance assumes the use of pre-adder.
3. Floating-point performance is IEEE-754 compliant single-precision.
4. Quad-core ARM Cortex-A53 hard processor system not available in Stratix 10 MX devices.
5. A subset of pins for each package are used for high-voltage 3.0 V and 2.5 V interfaces.
6. All data is preliminary and subject to change without prior notice.

656,32,312,0,96 Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, E-Tile transceiver count and H-Tile transceiver count.

Indicates pin migration path.