## INTEL® CYCLONE® 10 LP FPGAs PRODUCT TABLE

<table>
<thead>
<tr>
<th>PRODUCT LINE</th>
<th>10CL006</th>
<th>10CL010</th>
<th>10CL016</th>
<th>10CL025</th>
<th>10CL040</th>
<th>10CL055</th>
<th>10CL080</th>
<th>10CL120</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resources</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic elements (LEs)</td>
<td>6,000</td>
<td>10,000</td>
<td>16,000</td>
<td>25,000</td>
<td>40,000</td>
<td>55,000</td>
<td>80,000</td>
<td>120,000</td>
</tr>
<tr>
<td>M9K memory blocks</td>
<td>30</td>
<td>46</td>
<td>56</td>
<td>66</td>
<td>126</td>
<td>260</td>
<td>305</td>
<td>432</td>
</tr>
<tr>
<td>M9K memory size (Kb)</td>
<td>270</td>
<td>414</td>
<td>504</td>
<td>594</td>
<td>1,134</td>
<td>2,340</td>
<td>2,745</td>
<td>3,888</td>
</tr>
<tr>
<td>DSP Blocks (18 x 18 multipliers)</td>
<td>15</td>
<td>23</td>
<td>56</td>
<td>66</td>
<td>126</td>
<td>156</td>
<td>244</td>
<td>288</td>
</tr>
<tr>
<td>Phase-locked loops (PLL)</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>/O and Architectural Features</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Global clock networks</td>
<td>10</td>
<td>10</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Maximum user I/O pins</td>
<td>176</td>
<td>176</td>
<td>340</td>
<td>150</td>
<td>325</td>
<td>321</td>
<td>423</td>
<td>525</td>
</tr>
<tr>
<td>Maximum LVDS channels</td>
<td>65</td>
<td>65</td>
<td>137</td>
<td>52</td>
<td>124</td>
<td>132</td>
<td>178</td>
<td>230</td>
</tr>
<tr>
<td>Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, LVDS Pairs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M164 pin (8 mm x 8 mm, 0.5 mm pitch)</td>
<td>101,26</td>
<td>87, 22</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>U256 pin (14 mm x 14 mm, 0.8 mm pitch)</td>
<td>176, 65</td>
<td>176, 65</td>
<td>162, 53</td>
<td>150, 52</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>U484 pin (19 mm x 19 mm, 0.8 mm pitch)</td>
<td>340, 137</td>
<td>325, 124</td>
<td>321, 132</td>
<td>289, 110</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E144 pin (22 mm x 22mm, 0.5 mm pitch)</td>
<td>88, 22</td>
<td>88, 22</td>
<td>78, 19</td>
<td>76, 18</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F484 pin (23 mm x 23 mm, 1.0 mm pitch)</td>
<td>340, 137</td>
<td>325, 124</td>
<td>321, 132</td>
<td>289, 110</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F780 pin (29 mm x 29 mm, 1.0 mm pitch)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>423, 178</td>
<td>525, 230</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. LE counts valid in comparing across Intel devices, and are conservative vs. competing FPGAs.
2. This includes both dedicated and emulated LVDS pairs.
3. All data is correct at the time of printing and may be subject to change without prior notice. For the latest information, please visit www.altera.com.

* Other marks and brands may be claimed as the property of others. See Trademarks on intel.com for full list of Intel trademarks or the Trademarks & Brands Names Database.