Quartus II Software Questions & Answers

1. **What are the main new features and enhancements included in Quartus® II design software version 6.0?**
   Quartus II software version 6.0 delivers the highest productivity for programmable logic and structured ASIC designs. New in this release, the TimeQuest timing analyzer is the first timing analysis tool from an FPGA vendor to provide comprehensive native support for the industry-standard Synopsys Design Constraint (SDC) timing format. This ASIC-strength tool enables users to create, manage, and analyze designs with complex timing constraints, such as clock multiplexed designs and source synchronous interfaces, and to quickly perform advanced timing verification. In addition, version 6.0 includes an expanded team-based design environment with a project manager interface for managing resource and timing budgets at the top-level design.

2. **What are the additional productivity features and enhancements included with Quartus II software version 6.0?**
   Additional productivity features and enhancements beyond the TimeQuest timing analyzer include:
   
   - **Support for SystemVerilog** – Quartus II software version 6.0 allows faster register transfer level (RTL) implementation by supporting design constructs of the popular IEEE 1800-2005 Standard SystemVerilog syntax hardware description and verification language.
   - **Enhanced I/O pin planner** – Quartus II software version 6.0 includes I/O pin planner enhancements for easier integration of Altera® intellectual property (IP) and for simpler pin assignments.
   - **Expanded board-level design support** – Quartus II software version 6.0 offers HSPICE models of single-ended I/O for Stratix® II FPGA devices for more efficient board modeling.

3. **How does Quartus II software performance compare with competing products?**
   Quartus II software offers designers a full speed grade advantage for high-density 90-nm designs and up to a three speed grade advantage for low-cost 90-nm designs compared to the nearest competitor. For more information, visit [www.altera.com/alterazone](http://www.altera.com/alterazone).

**TimeQuest Timing Analyzer Tool**

4. **What is the TimeQuest timing analyzer tool?**
   TimeQuest is the first ASIC-strength timing analysis tool from an FPGA vendor to provide comprehensive native support for the industry-standard Synopsys Design Constraints (SDC) timing format. TimeQuest timing analyzer enables users to create, manage, and analyze complex timing constraints, such as clock multiplexed designs and source synchronous interfaces, and to quickly perform advanced timing verification. TimeQuest timing analyzer is available in Quartus II software version 6.0 subscription edition.
5. Who should use the TimeQuest timing analyzer?
Altera recommends the use of TimeQuest timing analyzer to ASIC engineers who are already familiar with the SDC format.

6. When should the new TimeQuest Timing Analyzer tool be used?
Altera recommends the use of the TimeQuest timing analyzer to FPGA design engineers designing source synchronous or multi-frequency interfaces, or to those already familiar with the SDC format. By adopting the new timing analyzer, designers will have more control over fine-tuning their timing constraints and will be able to achieve timing closure faster.

7. Which Altera device families does the TimeQuest timing analyzer tool support?
TimeQuest timing analyzer supports the following devices from Altera:
- Low-cost MAX® II CPLDs
- Low-cost Cyclone™ series FPGAs
- High-density Stratix series FPGAs
- HardCopy® II structured ASICs

8. What are the benefits of the TimeQuest timing analyzer tool?
The TimeQuest timing analyzer in Quartus II software enables thorough timing analysis of high-performance FPGA designs. Benefits to designers using the tool include:
- **Native SDC support** - Designers leverage a powerful industry-standard timing constraint format and achieve a higher degree of productivity due to use (and re-use) of SDC, $T_{cl}$-based scripts.
- **Fast on-demand and interactive data reporting** - Saves time and enables designers to request more detailed timing analysis only on critical paths. A powerful GUI reports the timing analysis data in an intuitive, easy-to-understand graphical format and complements fast, on-demand data reporting, further enhancing productivity.
- For HardCopy II structured ASICs, TimeQuest timing analyzer has the built-in precision and resolution necessary to automatically account for rise/fall timing characteristics.

9. Why is Altera introducing a new static timing analyzer?
As FPGAs become faster and achieve higher densities, they increasingly replace ASICs for complex designs and applications. This trend stresses the limits of traditional FPGA timing analysis tools, affecting designers’ productivity. TimeQuest timing analyzer resolves this dilemma with native SDC support, allowing designers to easily specify complex timing relationships among design signals and reach timing closure sooner.

10. Why is Altera using the SDC format in its TimeQuest timing analyzer tool?
The SDC timing constraints format provides an accurate, comprehensive, and concise modeling of complex timing relationships among design signals. SDC is an industry-standard format broadly adopted by ASIC engineers. Through the Synopsys TAP-in Program, Altera developed TimeQuest’s SDC-compliant front-end. Now, FPGA and
structured ASIC designers can constrain timing paths more accurately and get a fast, reliable ASIC prototype cycle with tools from Altera and Altera partners.

11. Are Quartus II software users required to use the TimeQuest timing analyzer?
   No. Designers can continue to use traditional FPGA timing analysis methodology with the Quartus II software classic timing analyzer.

12. Can Quartus II software users still use Synopsys’ PrimeTime to perform timing analysis?
   Yes. Quartus II software continues to fully support Synopsys’ PrimeTime.

13. Will the Quartus II classic timing analyzer and the TimeQuest timing analyzer deliver the same results?
   Under normal conditions, Quartus II classic timing analyzer and TimeQuest timing analyzer will produce consistent timing analysis results. Different results can occur if timing constraints differ, or if designers enable advanced features in the TimeQuest timing analyzer (such as rise/fall analysis for HardCopy II structured ASICs).

Altera recommends using a timing analysis tool when designing Altera devices. Switching timing engines between compilations will cause normal fitter variations, possibly resulting in differing timing results.

14. Will Altera maintain support for its classic timing analyzer?
   Yes. Altera recognizes that many Quartus II software users are comfortable with the classic timing analyzer and will continue to support it.

15. Which timing analyzer should designers use for timing sign-off of their FPGA designs?
   Both Quartus II classic timing analyzer and TimeQuest timing analyzer can be used for timing sign-off.

Additional Quartus II Version 6.0 Features

16. What is the Quartus II software's incremental compilation technology?
   Introduced in Quartus II software version 5.0, incremental compilation enables designers to divide designs into physical and logical partitions for synthesis and fitting (place-and-route). Designers using incremental compilation can reduce design compile time by up to 70 percent and reach design timing closure more efficiently. This feature supports block-based design, which allows the designer to preserve the performance of specified blocks while other blocks are undergoing optimization. Incremental compilation also enables top-down and bottom-up design flows, as well as a team-based design methodology.

17. What is the expanded team-based design feature introduced in Quartus II software version 6.0?
   Altera’s expanded team-based design feature includes a project manager interface for managing device resource and timing budgets. The project manager interface enables the
project lead to subdivide the project in a way that will eliminate resource conflicts (I/Os, memory, DSP blocks, etc.) when design blocks are combined at the top level. Designed for use with large or geographically dispersed teams, the new feature allows design teams to more efficiently collaborate in the design of high-density devices. The project manager interface benefits the single engineer using a bottom-up design methodology to manage larger and more complex FPGA-based designs. The new feature builds upon the incremental compilation design features introduced in Quartus II software version 5.0.

18. What’s new in the LogicLock™ feature?
Quartus II software version 6.0 includes a LogicLock enhancement called “LogicLock Membership Resource Filter.” This feature enhances design productivity by automating the process of excluding design elements of certain resource types (such as DSP elements, M4K memories, etc.) from a LogicLock region.

19. What SignalTap® II enhancements have been made in Quartus II software version 6.0?
- SignalTap II now includes a power-up auto trigger feature allowing users to perform on-chip debugging immediately after device configuration.
- The MATLAB interface now includes a native SignalTap II MEX function allowing SignalTap II to perform real-time, high-speed data acquisitions and present the data in the native MATLAB matrix format.
- Quartus II software now includes a Nios® II CPU SignalTap disassembly plug-in. The plug-in increases system-level debugging productivity by assisting the “tapping” of defined sets of Nios II nodes and by defining mnemonics for the Nios II CPU. The mnemonics make it easy to define trigger conditions for the processor and to represent captured data as Nios II instruction code.

General Q&A

20. What is Altera’s Quartus II design software?
Altera’s Quartus II design software is the industry’s first and only design tool to offer a unified design flow for the development of FPGAs, CPLDs, and structured ASICs. Quartus II design software accelerates performance, boosts productivity, and easily addresses potential design delays such as late-arriving, post place-and-route design changes.

21. How can a designer learn more about Quartus II software features and supported design flows?
Altera provides various avenues for designers to receive Quartus II technical information and training:

Quartus II Online Demonstrations – Demonstrations that provide the easiest way to learn about the latest Quartus II software features and design flows. These online demonstrations are available here: www.altera.com/quartusdemos

Introduction to Quartus II Manual – Overview of Quartus II software features and design flows. New Quartus II users can become productive quickly by
reading the “Introduction to Quartus II” manual. The manual can be downloaded at: www.altera.com/literature/lit-qts.jsp

**Quartus II Handbook** – Quartus II software users are recommended to access the Quartus II Handbook, a comprehensive software documentation that can be downloaded from: http://www.altera.com/literature/lit-qts.jsp

**Quartus II Instructor-Led Training Classes** – Free recordings of high-quality, instructor-led online training classes to learn about Quartus II features and design flows. For an updated list of the available courses please refer to: https://mysupport.altera.com/etraining/

**Quartus II Tutorials** – Tutorials included in the Quartus II software and Quartus II Web Edition software.

### 22. What is an Altera software subscription?

Altera’s software subscription program simplifies the process of obtaining Altera design software by consolidating development software products and maintenance charges into one annual fee. The annual subscription for the Altera design software is $2,000 for a node-locked personal computer (PC) license; subscriptions are also available to support other operating systems.

Altera’s Quartus II subscription edition design software includes the SOPC Builder system generation and integration tool, Mentor Graphics® ModelSim®-Altera software, Altera’s IP Base Suite including nine of the most popular IP cores (DSP, memory controllers, and Gigabit Ethernet MAC cores), perpetual licenses for several popular Altera MegaCore® IP functions, the MegaCore IP Library CD including OpenCore® Plus editions of all Altera MegaCore design-ready IP functions, the Nios II Embedded Design Suite CD, and 12 months of software upgrades.

### 23. What is the difference between Quartus II Web Edition software and the Quartus II software included in subscription products?

Quartus II Web Edition software includes most of the features included in the Quartus II software subscription edition and everything customers need to design for Altera’s latest CPLD and low-cost FPGA families. Quartus II Web Edition also includes support for entry-level members of Altera’s high-density FPGA families. More information is available at www.altera.com/products/software/products/quartus2web/features/sof-quarweb_features.html

### 24. Is the Quartus II software included in Altera development kits different from the Quartus II software included in Altera software subscriptions?

The Quartus II development kit edition (DKE) software and the Quartus II subscription edition software are equivalent in performance and functionality. Several differences exist in licensing and bundled IP. Altera’s Quartus II subscription edition offers access to upgrades for one year and perpetual software use. The Quartus II development kit edition includes access to upgrades along with software use for one year only. At the end of the year, customers can upgrade their development kit edition to the subscription edition at a discounted price, or use the free web edition version. Altera’s IP Base Suite, including
nine of the most popular IP cores (DSP, memory controllers, and Gigabit Ethernet MAC cores), is available only in the Quartus II subscription edition software.

25. Is the Mentor Graphics ModelSim-Altera edition included with the Quartus II software?
Mentor Graphics ModelSim-Altera software is included with Altera software subscriptions and can be licensed for the Windows, Solaris, or Linux platforms to support either VHDL or Verilog hardware description language (HDL) simulation. Currently, the ModelSim-Altera edition is not available to web edition users. Mentor Graphics ModelSim-Altera can also be downloaded from www.altera.com.

26. Quartus II software version 6.0 is available for which operating systems (OSs)?
Quartus II software version 6.0 is available on Windows XP, Windows XP x64, Windows 2000, Red Hat Linux Enterprise WS 3.0 and 4.0, and Solaris 8 and 9. Additionally, Quartus II 6.0 supports native 64-bit operation on Red Hat Linux Enterprise and on Solaris Operating Systems.

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