Nios II C2H Compiler Press FAQ

General
Q: What is the Nios® II C-to-Hardware Acceleration Compiler?
A: The Altera® Nios II C-to-Hardware Acceleration Compiler (Nios II C2H Compiler) is a productivity tool for Nios II users that can substantially increase the performance of their embedded software by automatically converting performance-critical C language subroutines into hardware accelerators and integrating them into FPGA-based Nios II subsystems. More information can be found on the Altera web site at http://www.altera.com/c2h.

Q: How can developers benefit by using the Nios II C2H Compiler?
A: Traditionally, embedded developers have had few options for accelerating performance, particularly near the end of a design cycle, outside of buying a faster processor or hand-tuning assembly language subroutines. While these methods can be used effectively, the tradeoffs in additional cost, increased power consumption, longer development time and reduced design flexibility are frequently unacceptable. The Nios II C2H Compiler gives developers another option: boost the performance of their existing software using the resources of the FPGA. The Nios II C2H Compiler generates hardware accelerators that can compute more per clock cycle than sequentially executed software code, meaning that developers can boost their systems’ performance without increasing processor clock frequency. By generating accelerators automatically, the Nios II C2H compiler eliminates the time-consuming process of developing acceleration logic by hand, reducing design time from weeks to minutes.

Q: How does the Nios II C2H Compiler work?
A: The Nios II C2H Compiler maps ANSI C constructs directly to RTL. For example, an addition operator (+) in C code is translated into an adder circuit in RTL, a pointer dereference is converted into a memory master and a while loop is converted into a state machine. The output is a hardware accelerator that shows up as an SOPC Builder component in clear-text VHDL or Verilog. The Nios II C2H Compiler heavily leverages the Avalon® interconnect fabric generated by SOPC Builder to provide high-bandwidth access to the processor’s memory subsystem. From the software perspective, the Nios II IDE performs all the necessary system connectivity and library linking to maintain identical functionality.

Q: Why is Altera providing this tool?
A: Altera is providing the Nios II C2H Compiler to:

• Leverage Altera’s system-level infrastructure to deliver Nios II C code performance improvements across a broad range of applications.
• Address the performance needs of the increasing number of embedded system designers choosing FPGAs as their processing platform.
• Support the large base of Nios II processor users who are eager for tools to simplify the creation of hardware acceleration logic.
• Give developers another way to exploit the inherent flexibility advantages of FPGAs and adapt to late-changing design requirements.

Q: What is the Nios II processor?
A: The Nios II embedded processor is a general-purpose 32–bit RISC CPU optimized for programmable logic and system-on-a-programmable-chip (SOPC) integration. With over 15,000 kits shipped and the world’s top 20 OEMs already using the Nios II processor, the Nios architecture is the most popular configurable soft processor available today.

Q: What is the SOPC Builder system development tool?
A: SOPC Builder is a powerful system development tool for creating systems based on processors, peripherals and memories. SOPC Builder enables users to define and generate a
complete system on a programmable chip (SOPC) in much less time than using traditional, manual integration methods. SOPC Builder is an exclusive Quartus® II software tool and is available to all Altera customers. Using SOPC Builder, FPGA designers specify the system components in a graphical user interface (GUI), and SOPC Builder generates the interconnect logic automatically. SOPC Builder outputs HDL files that define all components of the system, as well as a top-level HDL design file that connects all the components together.

SOPC Builder:
- Integrates off-the-shelf intellectual property (IP) from Altera or Altera Megafuction Partners Program (AMPP℠) Partners.
- Enables users to create their own reusable custom components to include in their systems.
- Generates hardware description language (HDL), building an interconnect fabric optimized for the requirements of each system.
- Outputs system test bench suites.

Q: What is the Avalon interconnect fabric?
A: The Avalon interconnect fabric is a true, nonblocking interconnect, automatically created by SOPC Builder, that supports multiple simultaneous master-slave transactions and therefore delivers dramatic improvements in overall system performance compared to traditional shared media bus structures. The Avalon interconnect fabric requires minimal FPGA resources and supports the following:
  - Simultaneous multiple master operation
  - Up to 4 Gbytes of address space
  - Synchronous interface
  - Built-in address decoding
  - Read and write transfers with latency
  - Streaming transactions
  - Dynamically sized peripheral interface
  - Multiple clock domains
  - Pipelined operation

Q: Is the Nios II C2H Compiler a general-purpose C-to-gates design tool?
A: No, Altera specifically designed the Nios II C2H Compiler to accelerate user-selected Nios II C code functions. It is not intended to convert entire C code applications into hardware designs.

Q: Can developers use the Nios II C2H Compiler for processors other than Altera’s Nios II processor?
A: No, the tool currently supports only the Nios II processor.

Q: What is the relationship between the Nios II C2H Compiler and Altera’s EDA partners in the ESL space?
A: The Nios II C2H Compiler is useful for Nios II developers who want to accelerate software performance by adding hardware accelerators to their designs. Altera’s Electronic System Level (ESL) partners provide tools that are useful for both general C-based design flows as well as for accelerating Nios II code through hardware acceleration. These ESL tools provide FPGA designers a choice in how they write code, hardware scheduling, efficiency and system design flows. The C2H compiler adds another option for Nios II developers that complements existing solutions from Altera’s ESL partners.

Q: Which of Altera’s EDA partners generate SOPC Builder-ready components today?
A: Celoxica and Impulse Accelerated Technologies tools currently create SOPC Builder-ready IP cores from C language code. We fully expect the opening of Altera’s application programming interfaces (APIs) to help stimulate support for other ESL partners in the future.
Q: Which FPGA families does the Nios II C2H Compiler support?
A: The Nios II C2H Compiler has the same device support as the Nios II processor: the Cyclone™
and Stratix® series of FPGAs, as well as HardCopy® structured ASICs.

Developing With the Nios II C2H Compiler

Q: What does “hardware accelerator” mean?
A: Hardware accelerators are dedicated blocks of logic designed to offload specific tasks from the
embedded software application. They are implemented in Verilog or VHDL. A broad range of
complex mathematic operations run faster and more efficiently when implemented in a fixed-
function hardware circuit versus a general-purpose CPU.

Q: Which ANSI C constructs does the Nios II C2H Compiler support?
A: The Nios II C2H Compiler supports the ANSI C standard, including all data types, operators,
control-flow and looping constructs, macros, function calls, and pointer and array access.

Q: Are there any ANSI C constructs the Nios II C2H Compiler does not support?
A: The initial release of Nios II C2H Compiler does not support floating point operations, recursive
routines or GOTO/LABEL statements.

Q: What kind of performance boost should developers expect to get with the Nios II C2H
Compiler?
A: Performance results vary depending on several factors (including algorithm implementation
and coding style); however, the Nios II C2H Compiler can deliver performance between 10 and
45 times greater than nonaccelerated software.

Q: How much logic does the Nios II C2H Compiler generate? What is the impact on the size of a
design?
A: There is a direct trade-off between performance boosts and increased logic usage. Many
mathematical algorithms translate well into hardware on the FPGA. Logic generated by the Nios II
C2H Compiler is strongly dependant on the coding style of the input C functions. For optimal
results, see the Nios II literature page for details on coding style and usage guidelines.

Q: Can developers add multiple accelerators to one design?
A: Yes, the only limit to the number of accelerators that a developer can add to a design is the
capacity of the targeted FPGA device. Practically speaking, there will generally only be a few
software subroutines that are the performance bottlenecks of the system and thus ideal
candidates for acceleration.

Q: Will developers have to rewrite their code to use the Nios II C2H Compiler?
A: While developers will not have to rewrite code to use the Nios II C2H Compiler, legacy C
software may not have been written in a way that most effectively translates to hardware. The
Nios II C2H Compiler will convert any ANSI C software code to hardware, but results will improve
dramatically by following the recommended coding style usage guidelines.

Q: Can developers switch between the hardware or software implementations of their algorithms?
A: Yes, the Nios II IDE lets developers easily add or remove functions from the Accelerated
Functions view. Once a software routine has been selected for acceleration, developers can still
opt to run their applications using either the software or hardware implementations. Developers
often use this feature to verify that the Nios II C2H Compiler-generated hardware accelerator is
functionally identical to the original software algorithm.

Q: Does the Nios II C2H Compiler require users to have the Quartus II design software installed?
A: Yes. The Nios II C2H Compiler generates RTL code to replace certain software routines in an
application. This RTL relies on the SOPC Builder tool for integration into the Nios II system and
the Quartus II software for synthesis and fitting into the FPGA. These are both essential components. The Quartus II software is available for download at www.altera.com/download.

Availability and Licensing
Q: When will the Nios II C2H Compiler be available?
A: The Nios II C2H Compiler has been shipping to beta customers since October 2005; the official product release will be in May of 2006.

Q: How can developers get the Nios II C2H Compiler?
A: The Nios II C2H Compiler will be delivered as an integrated plug-in to the Nios II IDE. The Nios II IDE is included with Nios II Embedded Design Suite, which ships with all Nios II development kits and the Quartus II design software, and is available for download at www.altera.com/niosdownload.

Q: How much does the Nios II C2H Compiler cost?
A: The Nios II C2H Compiler costs US$2,995 per license seat. Additionally, it requires an active Nios II subscription, available for US$495 per seat. The Nios II C2H Compiler license includes 12 months of updates, and an annual maintenance subscription will be available for US$1,495 per seat.

Q: What is the licensing model for the Nios II C2H Compiler?
A: Developers who purchase the Nios II C2H Compiler receive a perpetual license to develop and ship systems including Nios II C2H Compiler-generated hardware accelerators. The royalty-free license applies to designs deployed in Altera FPGAs or structured ASIC devices. After purchasing the tool, customers will receive a text license file that will be required in order to generate a shippable system.

Q: Can developers try out the Nios II C2H Compiler before they buy it?
A: Yes, interested developers should contact their local Altera representative for a free evaluation version of the Nios II C2H Compiler.

Q: Are developers required to purchase a Nios II license seat to use Nios II C2H Compiler?
A: In order to license the Nios II C2H Compiler, developers must have an active Nios II subscription.

Q: Do tools like the Nios II C2H compiler exist from other FPGA providers?
A: Currently Altera is the only FPGA provider with integrated tools for accelerating C code running on an embedded processor within the FPGA.

Q: Did Altera develop the Nios II C2H Compiler internally?
A: Yes, Altera developed the Nios II C2H compiler internally, a process that has taken several years effort, and has several patents pending on this unique technology.