OTN Family | 100G Muxponder |TPO404 + PQ60T

Altera's OTN SoftSilicon® Family provides a complete family of optical network processors for metro/core OTN and packet networks covering applications from network interfaces over transponders and muxponders to large OTN cross connect or Packet-Optical Transport Systems (P-OTS).

The Altera SoftSilicon® solution provides maximum performance while optimizing customers' time-to-market, flexibility, risk profile, and cost-over-lifetime.

Family Key Features

- All OTN networking applications covered
- Latest OTN/packet standards supported
- Maximum flexibility provided
- Low risk for system vendors and end users
- Low development cost and total cost of ownership
- 2.5 Gbps – 100 Gbps bandwidth
- G.709 OTN mapping, multiplexing, cross-connection, framing and FEC
- Client ports configurable to any rate and any protocol
- Support of ODU0 and ODUflex
- Built-in ODU cross connect for efficient sub-wavelength networking
- Stand-alone and switch-fabric applications
- Maximum flexibility and low risk for system vendors and end users
- Advanced and easy-to-use software API

All Applications

Altera provides standard solutions for all applications in the packet optical space, ranging from simple, but efficient, framer/mapper interface components over stand-alone transponder and muxponder systems to 100G capacity, high density line cards on ODU cross connect and P-OTS.

Fastest time-to-market

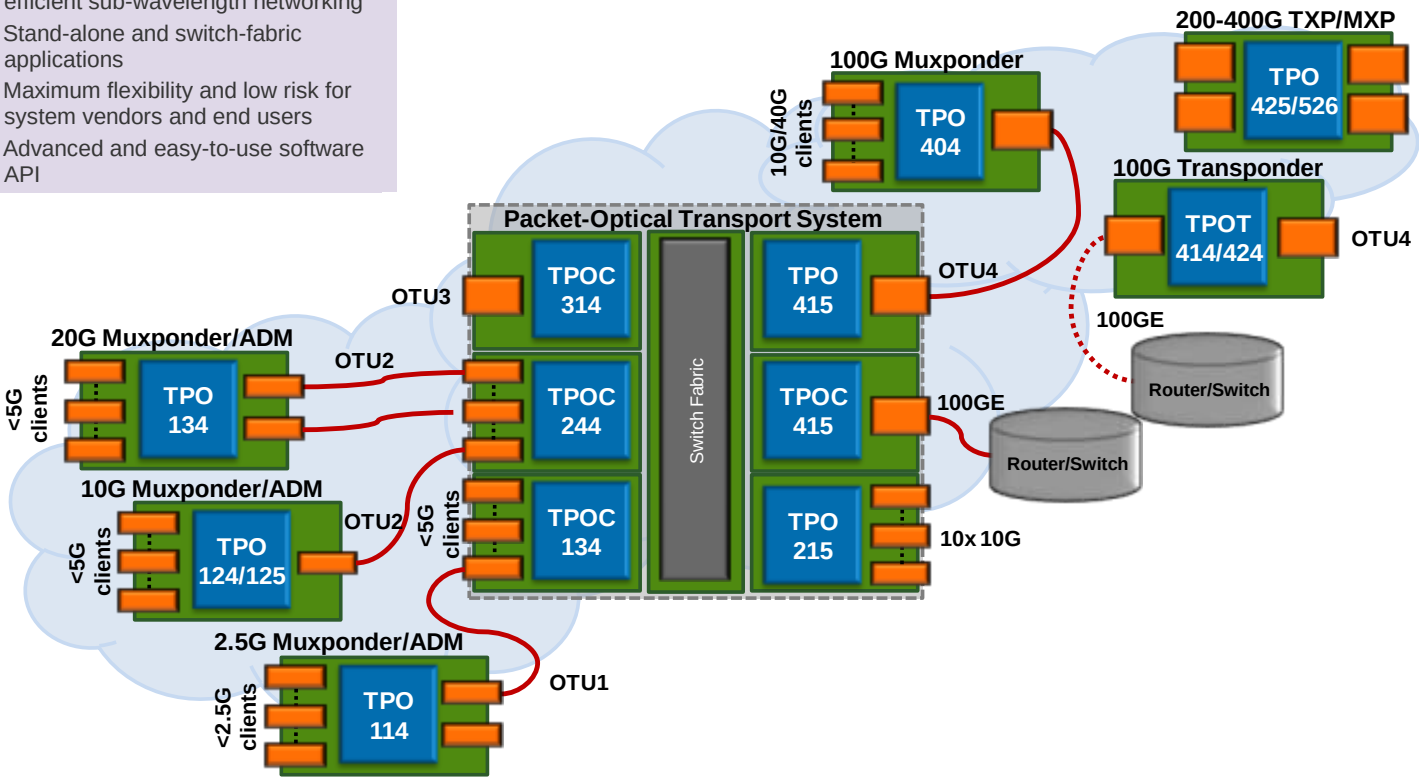
The Altera SoftSilicon® model with standard devices with a well-defined set of features, pin-out and software API validated on reference hardware guarantees shortest time to market.

Lowest Risk

Because SoftSilicon® devices have been built and validated on reference platforms that closely resemble the target application they minimize the development risk for system providers. The FPGA platform mitigates the risk from new or changing requirements from end-customers or standardization bodies.

Low Development and Maintenance Cost

Altera provides an easy-to-use unified software API for the various solutions even when chip sets are used. This makes it efficient for software teams to integrate their solutions into the system software and makes software maintenance much easier, particularly if hardware solutions are migrated to more integrated implementations and new process nodes over time.



TPO404 + PQ60T | 100G Muxponder

Specifications

Line Interface (TPO404)

- OTL4.10 OTU4

Client Interface (PQ60T)

- OTL3.4 / SFI-5.1 OTU3
- XLAUI 40GE
- STL256.4 OC-768 / STM-256
- SFI / XFI OTU2,10GE, OC-192, STM-64, 8GFC, 10GFC

Client Mapping Function

- Supports LAN, WIS and all five 10GE mapping modes outlined in ITU G.Sup43
- Supports 8G/10G FC, 40GE and OC-768/STM-256 mapping
- Supports transparent mappings of 10G and 40G SONET/SDH clients

FEC Client Side OTU2/OTU3

- G.709, G.975.1, I.4 and G.975.1, 1.7 FEC

FEC Line Side OTU4

- 6dB/7% G.709 RS

OH Processing

- Full OTN and SONET/SDH (WIS compliant) overhead monitoring with overhead drop/insert support

CPU Interface

- PCI-E or parallel

Solution

The 100G muxponder solution is a highly efficient combination of the TPO404 100G multiplexer and framer and the AppliedMicro PQ60T 10-40G client mapper and framer.

Function

The 100G muxponder will multiplex any combination of 10G and 40G client signals into a 100G OTN signal (OTU4).

The muxponder interfaces directly to optical modules at both client and line side.

In direction from client side to line side 10G client signals are mapped into ODU2/2e containers. 40G client signals are mapped into ODU3 containers.

Client side signals may also be OTU2/2e signals or OTU3 signals. For these signals the muxponder will do error correction based on the forward error correction (FEC) parity information embedded in the signal overhead. There is support for both the G.709 Read Solomon FEC scheme with a net coding gain of around 6dB and the G.975.1 I.4 and I.7 enhanced FEC schemes with more than 8dB of coding gain.

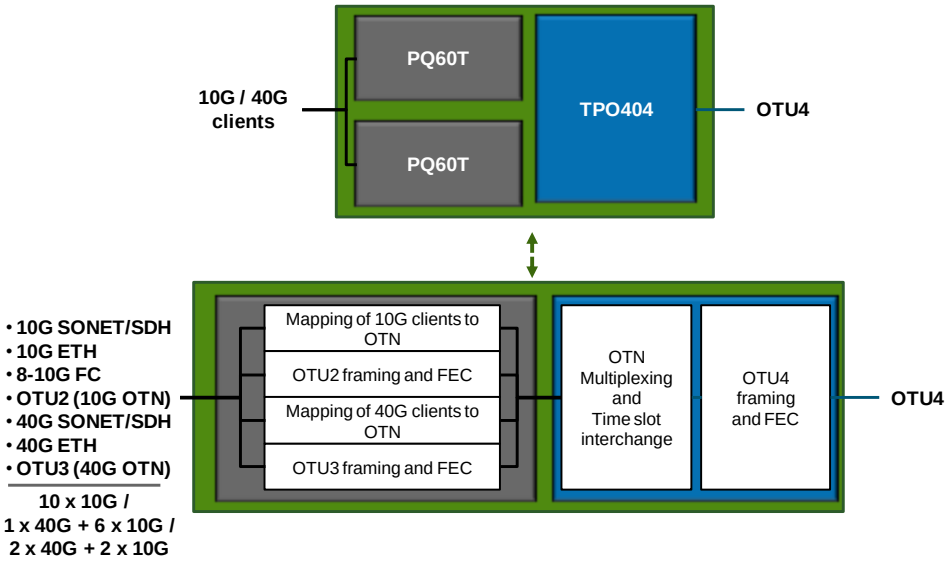
Following the FEC termination the OTU2 and OTU3 framing and overhead information will be terminated leaving the embedded ODU2/2e and ODU3 containers.

The resulting ODU2/2e and ODU3 containers are subsequently multiplexed and mapped into an ODU4 container using GMP mapping where after overhead information, OTU4 framing and G.709 FEC is added. The line side interface is OTL4.10.

Coming from the line side the opposite actions are taking place. At the client egress side the muxponder will derive the original client clock for those clients that were mapped clock transparently on the ingress side and use this clock for transmission. For other clients a system clock will be used for transmission.

Driver Software

Altera delivers one common high level driver API software for the entire muxponder solution consisting of the TPO404 and the two PQ60T. This assures minimum software integration and maintenance effort for customers and makes the whole solution much less error prone. The software can be compiled to any OS.



Altera Corporation
101 Innovation Drive
San Jose, CA 95134
USA
www.altera.com

Altera European Headquarters
Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1494 602000

Altera Japan Ltd.
Shinjuku i-Land Tower 32F
6-5-1, Nishi-Shinjuku
Shinjuku-ku, Tokyo 163-1332
Japan
Telephone: (81) 3 3340 9480
www.altera.co.jp

Altera International Ltd.
Unit 11-18, 9/F
Millennium City 1, Tower 1
388 Kwun Tong Road
Kwun Tong
Kowloon
Hong Kong
Telephone: (852) 2945 7000
www.altera.com.cn