Dual BCH FEC IP Cores

General Features

- 8.39dB net coding gain at 10^-15 output BER
- 10G, 40G, or 56G rates, and variable rates in between
- Generic CPU interface for control and monitoring

Application Diagrams

Example Application: 40G

Receive System Side Interface Input Signals

- SFI-5 Tx Output External Signals
  - SPI-5 OTPs
  - SPI-5 Encoding
  - PRBS gen
  - OTN scrambler
  - OTN error injection
  - Dual BOC encoder
  - OTUK gen
  - ODUK gen
  - OPUK gen
  - PRBS gen

Transmit System Side Interface Input Signals

- SFI-5 Tx Output External Signals
  - GTP Lookbacks
  - Per Lane PRBS gen
  - SPI-5 Loopback
  - PRBS gen
  - OTN-AIS gen
  - SFI-5 Encoding
  - OTUK Framer
  - ODUK Monitor
  - OPUK Monitor
  - PRBS Monitor

Key Features

- IP core is smaller than BCH/RS EFEC with similar gain
- Supports for ASIC and FPGA implementations
- Ideal for 112G (2x56G) transport applications

Statistics:

- Corrected bits
- Corrected ones
- Corrected zeros
- Corrected codes
- Uncorrectable codes
Related Products
For additional information regarding Altera FOTN IP solution visit www.altera.com.

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For more information about this IP cores, please contact your Altera® sales representative or FAE, or visit www.altera.com.