

Altera wireless solutions

Simplify your 3GPP LTE channel card design cycle

Design for volume, design with agility

Altera's 3GPP Long-Term Evolution (LTE) portfolio of wireless solutions enables you to design your basestation applications with agility and for volume right from the start. Read on to learn more about our wireless reference designs. Visit www.altera.com/wireless for more information.

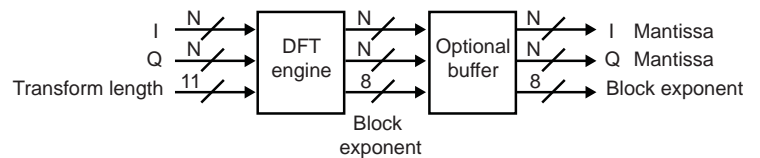
LTE IP and reference designs

Discrete Fourier transform (DFT)/inverse DFT (IDFT) reference design

Altera supplies the reference design as clear-text VHDL, including a fixed-point MATLAB simulation model.

- Supports all of the 34 transform sizes specified in the 3GPP LTE standard
- Supports run-time configuration on a block-by-block basis between the transform sizes
- User-defined inputs for specifying transform mode (DFT or IDFT) and internal bit widths
- Highly optimized design targeting efficient use of Stratix® II and Stratix III FPGA resources

DFT/IDFT

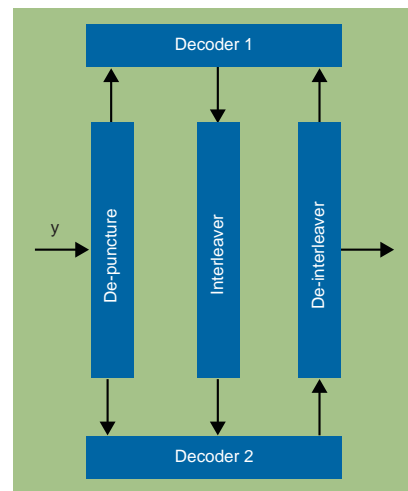


Turbo encoder/decoder reference design

Altera supplies the reference design as clear-text VHDL, including a bit-accurate C simulation model.

- Supports all 188 code blocks defined in LTE standard from 40 to 6,144 bits (run-time selectable)
- Supports run-time selection of #iterations and #soft bits
- Supports throughputs in excess of 100 Mbps
- Highly optimized design targeting efficient use of Stratix II GX and Stratix III FPGA resources

Turbo encoder/decoder

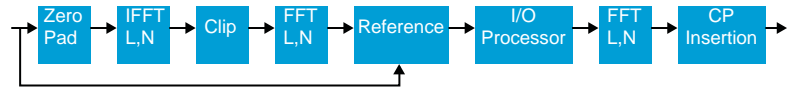


Crest factor reduction (CFR) reference design

Altera supplies the reference design as clear-text VHDL, including a MATLAB bit-accurate simulation model.

- Support for OFDM-based systems including WiMAX and 3GPP LTE
- Additional functionality includes OFDMA symbol modulation, digital upconverter (DUC) (4x interpolation), and cyclic prefix insertion
- Programmable mask and programmable error vector magnitude (EVM) budget
- Programmable channel bandwidths including 10 and 20 MHz
- Up to 5db peak-to-average power ratio (PAPR) improvement
- No receiver-side modification required

CFR

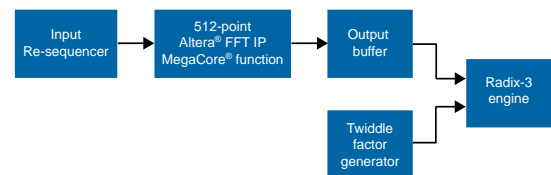


1536 fast Fourier transform (FFT)/inverse FFT (IFFT) reference design

Altera supplies the reference design as clear-text Verilog, including a MATLAB bit-accurate simulation model.

- Streaming 1,536-point FFT with natural input and output order
- Avalon® Streaming- (ST-) compliant interfaces without backpressure
- Fixed point I/O representation to maintain precision
- Transform direction (FFT/IFFT) specifiable on a per-block basis
- Verilog testbench and Tcl script provided for the ModelSim® simulator

1536 FFT/IFFT

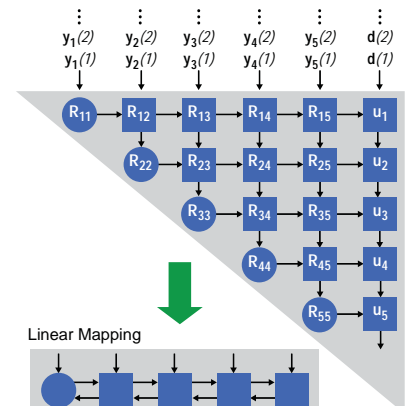


QR decomposition reference design

Altera supplies the reference design as clear-text VHDL, including a MATLAB bit-accurate simulation model

- Includes QR decomposition and back substitution
- Supports complex inputs with both fixed and floating point support
- Applications include matrix inversion, multiple-input multiple-output (MIMO) decoding, and digital predistortion
- Highly optimized design targeting efficient use of Stratix II and Stratix III FPGA resources

QR decomposition



Altera Corporation
101 Innovation Drive
San Jose, CA 95134
USA
www.altera.com

Altera European Headquarters
Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1 94 602 000

Altera Japan Ltd.
Shinjuku i-Land Tower 32F
6-5-1, Nishi-Shinjuku
Shinjuku-ku, Tokyo 163-1332
Japan
Telephone: (81) 3 3340 9480
www.altera.co.jp

Altera International Ltd.
2102 Tower 6
The Gateway, Harbour City
9 Canton Road
Tsimshatsui Kowloon
Hong Kong
Telephone: (852) 2945 7000

