



High Bandwidth, Low Power, and Low BER

Altera's 28-nm, Power-Efficient Transceivers

Altera® transceivers have a proven track record of meeting system bandwidth, power, and bit-error rate (BER) requirements. This technology leadership continues with our 28 nm Stratix® V FPGAs.

Our high-bandwidth and power-efficient Stratix V FPGAs give your products more reach, flexibility, and reliability. We also provide simulation tools to enable a faster design process so you can ship your products faster. In addition, our best-in-class transceivers are compliant with a range of protocols and come with a variety of transceiver signal integrity features to support backplane, optical module, and chip-to-chip applications.

High-Speed Serial Protocols

Standard	Electrical Serial Line Rate (Gbps)
OIF/CEI 28G-SR/VSR	25/28
16G Fibre Channel	14.025
IEEE 802.3ba 40G/100G 10GBASE-R/10GBASE-KR	10.3125
10G GPON/EPON	10
OIF SFI-S/SFI-5.2(40G)	9.95 to 11.1
10G Interlaken	10.6921
SONET/SDH OC-192 (10G / 40G)	9.95
SFP+	8.5 to 11.32
XFP	9.95328 to 11.32
OIF/CEI 11G-SR & LR	9.95 to 11.1
OTU2/OTU3/OTU4	10.709/10.7545/11.2
10G SDI	10.6921
QDR InfiniBand	10
PCI Express® 3.0/2.0/1.0 ¹	8/5/2.5
Interlaken	4.976 to 6.375
SRIO 2.0+	1.25, 2.5, 3.125, 5 to 6.25
CPRI 4.0+	0.6144, 1.2288, 2.4576, 3.072, 4.9152, 6.144
SATA 3.0/SAS 2.0	6
QPI	4, 4.8, 6.4, 8
HyperTransport™ 3.0+	0.4, 2.4, 2.8, 3.2
HighGig+, HighGig2+	3.75, 6.25
Fibre Channel (8G/4G)	8.5/4.25
OIF/CEI 6G-SR	4.976 to 6.375
XAUI	3.125
SFI-4.2(10G)/SFI-5.1(40G)	3.125

¹Hard intellectual property (IP)

Highest Bandwidth for Greater Reach

Stratix V FPGAs provide the highest system bandwidth with as many as 66 full-duplex transceiver channels with data rates of up to 14.1 Gbps, and 4 full-duplex transceiver channels with data rates of up to 28.05 Gbps.

You can clock each independent transmit channel using the following modules:

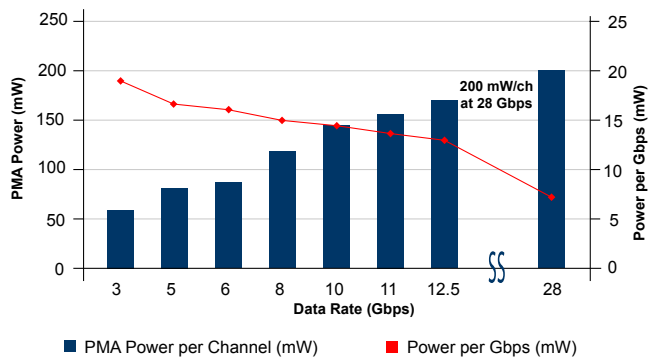
- An LC oscillator, which provides very low jitter in the sub-picoseconds range.
- A wide data range (600 Mbps - 12.5 Gbps) ring oscillator
- A new fractional phase-locked loop (fPLL) in the core fabric

Furthermore, you can derive reference clocks from off-chip oscillators. You can also generate the reference clocks on chip with the precise frequency synthesis capabilities of the new fPLLs. fPLLs synthesize multiple clock frequencies from a single reference clock source and replace multiple reference oscillators, including voltage controlled crystal oscillators (VXCOs), in multi-protocol or multi-rate applications.

Lowest Power for Increased Flexibility

Stratix V FPGAs deliver the highest system bandwidth at the lowest power consumption for a wide range of applications. Figure 1 shows the transceiver physical media attachment (PMA) power per channel for data rates of 6.5 Gbps up to 28.05 Gbps.

Figure 1: Transceiver PMA Power per Channel



Lowest BER for Better Reliability

Stratix V transceivers give you best-in-class system reliability with the lowest jitter. Transmit and receive advanced equalization capabilities fully support 10GBASE-KR backplanes at the lowest BER. The transceivers are on the outer edges of the chip. This protects the transceivers from core and I/O noise, which ensures optimal signal integrity.

Altera also provides the following tools to help you simulate and examine transceiver link quality:

- Transceiver HPSICE models and behavioral IBIS-AMI models. These enable you to achieve a higher level system circuit simulation for link analysis and board design
- Pre-emphasis and equalization link estimator (PELE). This provides you optimal transmitter and receiver equalization coefficients for jitter performance estimation to ensure that the high-speed serial link will interoperate at the target BER
- New EyeQ eye viewer. This completely reconstructs the vertical and horizontal eye opening for you after equalization and performs clock recovery in the receiver. You can use the EyeQ on-die instrumentation non-invasively to tune for ideal equalization coefficient settings or to debug a transceiver link when combined with dynamic reconfiguration

Transceiver Signal Integrity Features

Feature	Stratix V FPGA
Data rates	<ul style="list-style-type: none"> • 20 Gbps to 28.05 Gbps (GTB) • 600 Mbps to 14.1 Gbps (GXB)
Backplane support	<ul style="list-style-type: none"> • Up to 12.5 Gbps, including 10GBASE-KR
Optical module support	<ul style="list-style-type: none"> • XFP • Small form factor pluggable (SFP+) • Quad small form factor pluggable (QSFP) • CXP • CFP
Architecture	<ul style="list-style-type: none"> • Independent transmit and receive channels • Full PMA and physical coding sublayer (PCS) on all channels • Extensive hard PCS per channel, including 8b/10b, 64b/66b, and 64b/67b encoding
Receive clocking	<ul style="list-style-type: none"> • Analog PLL-based clock data recovery (CDR) per receive channel
Transmit clocking	<ul style="list-style-type: none"> • fPLL (up to 3.75 Gbps) • CMU (600 Mbps to 12.5 Gbps) • Programmable LC (3.25 Gbps to 14.1 Gbps and 20 Gbps to 28.05 Gbps)
Continuous time linear equalization (CTLE)	<ul style="list-style-type: none"> • Programmable 4-stage receive channel linear equalization for high-attenuation channels (up to 16 dB)
Decision feedback equalization (DFE)	<ul style="list-style-type: none"> • Receive channel 5-tap digital equalizer to minimize losses and crosstalk
Adaptive dispersion compensation engine (ADCE)	<ul style="list-style-type: none"> • Adaptive engine that automatically adjusts equalization to compensate for changes over time
PLL-based clock recovery	<ul style="list-style-type: none"> • Superior jitter tolerance versus phase interpolation techniques
Transmit equalization (pre-emphasis)	<ul style="list-style-type: none"> • Transmit channel driver 4-tap pre-emphasis and de-emphasis for protocol compliance under lossy conditions

Want to Dig Deeper?

Learn more about Stratix V transceiver technology by meeting with your local Altera sales representative or FAE, or visiting www.altera.com/stratixv

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