BCH/RS FEC IP Core

General Features
- Compliant with G.975.1 Annex 4
- 8.56dB net coding gain at 10-15 output BER
- 10G or 40G rates and variable rates in between
- Generic CPU interface for control and monitoring

Key Features
- Enables replacement of 1.4 ASSPs
- Support for ASIC and FPGA implementation

Statistics:
- corrected bits
- corrected ones
- corrected zeros
- corrected codes
- corrected blocks
- uncorrectable codes

Application Diagrams

Example Application: 40G

Receive System Side Interface Input Signals

Transmit System Side Interface Input Signals

175 Mhz
ll_te_sys_clk: The line transmit clock

175 Mhz
ll_rx_sys_clk: The line received clock derived from the transponder
Related Products
For additional information regarding Altera OTN IP products visit www.altera.com.

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For more information about this IP core, please contact your Altera® sales representative or FAE, or visit www.altera.com.