Accelerating applications on coprocessing platforms

Up to 100X faster performance, 90 percent less power

From processing stock trades to analyzing investment account data and performing matrix mathematics, your high-performance computing system is at the heart of your business. That's why you expect:

- The highest performance
- The lowest power consumption
- The most productive environment possible for anyone who uses or maintains the system
- And a price point that won't send your finance department into a tailspin

If you haven't already, it's a good time to consider FPGAs in your high-performance computing system. Today's coprocessing platforms using FPGAs are simpler to design and yield more powerful performance results than do traditional architectures.

Altera offers high-performance FPGAs that, in a coprocessing platform, accelerate algorithms and applications from 10X to 100X compared to traditional architectures, while reducing power consumption by as much as 90 percent. Along with our high-performance computing ecosystem partners, we're delivering the optimal mix of resources to help you gain the most value from your system investment.

Doubled performance level in floating point applications

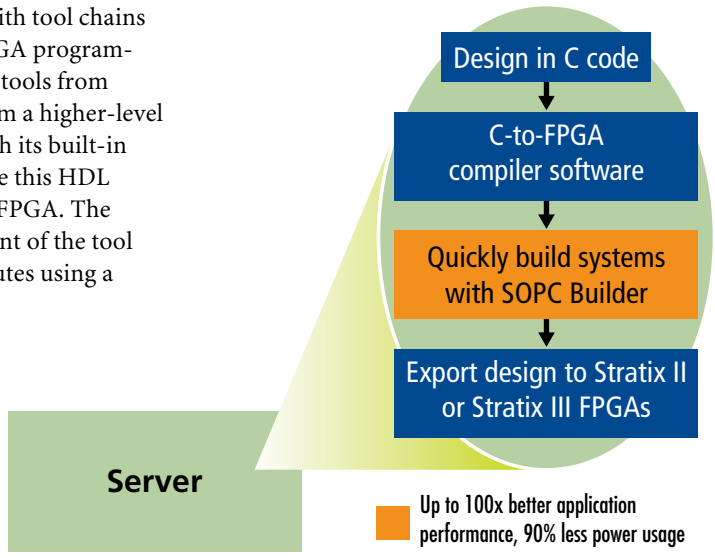
Many applications—including radar, bioscience, finance, matrix math, molecular dynamics, and seismic imaging—are increasingly using floating point data types for more accurate results. For these floating point applications, Altera® Stratix® II and Stratix III FPGAs offer double the performance of competitive solutions, thanks to their balance of logic elements (LEs) to multipliers.

Altera device	Sustained GFLOPS	Precision
Stratix II	14.9	Double
Stratix III	32.1	Double

Faster, simplified design process

Designing high-performance computing systems is made easy with tool chains that will take in C/C++ at the input and deliver the low-level FPGA programming file. You don't need to understand Verilog or VHDL. New tools from Altera's partners will create the design in HDL automatically from a higher-level software representation. Altera's Quartus II® software, along with its built-in system-on-a-programmable-chip tool – SOPC Builder – will take this HDL design and compile it to the actual hardware that will run in the FPGA. The design is optimized for the targeted hardware by every component of the tool chain. This process helps you to create custom hardware in minutes using a push-button approach.

C-to-FPGA design flow



Meet power, performance, and price goals

Because FPGAs can be programmed at any stage in the design cycle—even in the field—they present a very flexible solution for high-performance computing systems. Unlike ASICS, FPGAs can be altered when there are changes in specifications, algorithms, or industry requirements. Where you might require multiple ASICS—since each device is tied to only one function—you can consolidate functions onto a single FPGA. This saves board space, lowers power consumption, and increases system performance.

FPGA performance increases with each process generation. Parallelization—both in the hardware and in high-speed network and memory access—further enhances performance. In contrast, traditional processor-only models may not be able to keep up with increasingly demanding performance and power consumption requirements.

Highest-performance, lowest-power coprocessing accelerators

Develop your high-performance computing system with Altera's Stratix series FPGAs, which work seamlessly with Intel and AMD microprocessors. These FPGAs provide an optimal and efficient mix of high-performance digital signal processing (DSP) capabilities, easy to access on-chip memory, and best-in-class signal integrity.

- Stratix II FPGAs, based on a proven 90-nm process technology, have been in production for 2 years and offer excellent performance, signal integrity, and optimal power usage. Based on a revolutionary, patented, and efficient architecture, Stratix II devices provide a highly efficient core to match your design requirements.
- Stratix III FPGAs, based on a 65-nm process technology, combine the world's highest performance and highest density with the lowest possible power consumption. Available exclusively in Stratix III FPGAs, Programmable Power Technology allows users to maximize performance where needed in the design while operating in low-power mode in other blocks (memory, core, and DSP). As the industry moves to the DDR3 memory interface, look to our Stratix III FPGAs, the market's only such devices with DDR3 support to meet your high-bandwidth requirements while further lowering power consumption.

Collaborating to develop the right resource mix for you

Because no single supplier can provide all of the high-performance computing coprocessing resources a company needs, Altera partners with other leading companies. Our ecosystem provides the optimal mix of resources to accelerate your financial applications.

Want to dig deeper?

For more information or to discuss your high-performance computing environment, contact your local Altera FAE or sales representative for a meeting. Also, visit **www.altera.com/hpc**

Partner offerings in high-performance computing

Partner solution	Altera connection	Benefits
XtremeData XD2000i FPGA Coprocessor Module	Stratix III FPGAs	10X to 100X application acceleration and lower power consumption for Intel Xeon-based servers; module for Intel Xeon socket
XtremeData XD1000 FPGA Coprocessor Module	Stratix II FPGAs	Cost-effective FPGA acceleration platform for AMD Opteron servers, deployable in the densest blade systems; module for AMD Opteron socket
SRC Computers, SRC-7 series computing systems and CARTE	Stratix II FPGAs and Quartus II design software	Eliminates need for hardware design knowledge; delivers computing platform with high gate count, high bandwidth interconnect, and high bandwidth mass storage; plugs directly into a memory DIMM socket
Impulse Accelerated Technologies Impulse C	Compatible with Quartus® II design software, SOPC Builder, and Nios® II C-to-Hardware Acceleration (C2H) Compiler	Compiles C language applications into optimized FGPA logic, accelerating embedded algorithms by as much as 300X over traditional processor implementations

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